METROPHYSICS INC.

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ADVANCED TRANSDUCERS

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PHASE B: Design of a Digital Adaptor with Limit Storage for Transducers

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ADVANCED CHECKOUT TRANSDUCERS

1.0 INTRODUCTION

The results of METROPHYSICS, Inc.'s effort during Phase B of contract NAS 8-20515 are presented in this report. The objective of this effort was the design of a new adaptor for checkout transducers in preparation for the fabrication of a prototype model. The main features of the adaptor are:

1) It incorporates A/D conversion. It accepts a standard 0 to 5 V and converts it into a 10 bit binary number.
2) It provides limit storage and comparison. The measurand is continuously compared to limits of amplitude and rate of change, and whenever one of these limits is exceeded, a signal is produced indicating this event.
3) It permits random addressing. The adaptor, and therefore the channel in which it is used can be addressed in any desired sequence, or left silent.
4) It requires minimum cabling. A system employing one adaptor on each of its transducers requires only two input and one output lines, or wires, besides ground and power lines, for system interconnections.
5) It allows the stored limits to be changed at any time. The limits stored in the adaptor can be changed either remotely by programming the controlling unit, or locally by a special device.

The design uses integrated circuits throughout and is based on available MOS field effect transistor integrated circuit modules.

It is this type of integrated circuit which makes it possible to obtain an adaptor module compatible with the size of the average signal conditioners.

It is proposed to build an experimental system of 6 adaptors to demonstrate the feasibility of the concept of an adaptor for checkout transducers in real operation. Auxiliary equipment needed to this end is also described in this report.

2.0 BACKGROUND

Modern technology made it possible to use pulse code modulation telemetry with subsequent digital data handling extensively and to great advantage. The advantages offered by digital data processing are most fully realized when the desired information is converted to digital form as closely to its origin as possible. Ideally, in the information source itself. In isolated cases (on-off signal) this ideal is realized, but most information sources with which we are concerned here are analog in nature.

To improve the situation - at least in telemetry- the idea of developing a so-called digital transducer appeared.

At the same time the demand for more information increased, leading to more complex telemetry systems with many information carrying channels. It became apparent that much of the data thus acquired was actually redundant and could have been discarded without loss of pertinent information. This brought about various methods of reducing the data to be gathered or handled known as "data compression".

One way of achieving data compression is to restrict the range within which a data source is allowed to transmit information.

In the case of a transducer, for instance, one could store limits of amplitude and rate of change directly at the transducer and inhibit its output as long as none of these limits has been exceeded by the measurand.

It follows that a transducer featuring both digital output and data compression by limit storage, would be a highly desirable item.

Attempting to uncover a transducer design which would satisfy the above requirements, a survey of digital transducers was undertaken by MP/I. Only one concept was found that holds promise for developing a future family of digital transducers. Even in this case limit storage could not be accomplished easily.

With the above results in mind, an alternate solution - originally suggested by MP/I in its unsolicited proposal - was adopted: the digital adaptor with limit storage for transducers.

The digital adaptor falls short of the ideal but moves the analog to digital conversion as closely to the information source as presently feasible. Even with the advent of an ideal digital transducer, the usefulness of this concept will not be exhausted, for the limit storage and comparison circuits in their microminiaturized form are equally applicable whether the measurand is inherently digital or converted to digital form from its orginally analog form.

3.0 DESIGN CONSIDERATIONS

In the following, it is attempted to present the line of reasoning which lead to a concept of an adaptor for transducers which allows the use of standard analog transducers in multi-channel digital data acquisition systems. A system using such adaptors in connection with a control unit (computer), must offer certain advantages over conventional system in order to justify the higher cost per channel. The features which will make a system based on a digital adaptor superior to other systems are:

1) Information is provided by the adaptor in digital form.
2) Random addressing of each channel is possible.
3) Channels do not transmit information as long as they are not addressed or the information they are carrying is not pertinent.
4) Installation must be simple requiring a minimum of cabling.
5) The rate of data flow must be high enough to cope with the vast amount of information presented to the system.

An adaptor suitable for such a system must be small, provide data compression and be easy to install. It is also highly desirable that the concept on which it is based does not become obsolete too fast.

Recent advances in integrated circuit technology made the idea of a digital adaptor for transducers practical. The high function density of modern integrated circuit modules, especially of MOS field effect integrated circuits, make it possible to

obtain a package small enough to be compatible with modern telemeter packaging practices.

Such an adaptor must perform the following functions:

1) It must convert the measurand (output of a transducer) into a binary number of 9 to 10 bits (.2 to .1% resolution).
2) It must be capable of storing amplitude and rate of change limits imposed on the measurand.
3) It must be able to detect a condition in which the measurand had exceeded any of the limits and to indicate this event.
4) It must present the measurand in digital form to the control unit upon request (being "addressed").
5) It must allow the limits to be changed without interfering with its normal operation.

A concept of a digital adaptor which meets the above requirements is expounded in the following.

A system which uses the digital adaptor will require a control unit. This control unit will most likely be an electronic computer, programmed to accept information from the adaptors and to process it. In addition it will have to provide timing signals and to make decisions as to which channels are to be processed.

It should be pointed out that the timing regulating A/D conversion and limit monitoring could be done by each individual adaptor. However, no advantage would be gained. Only the size and cost of the adaptor would be increased, or some way of synch-

chronization between control unit and adaptor would have to be provided in either case.

The adaptor can be considered to be made up of two functional parts: an A/D converter and a special purpose computer.

Small A/D converters available today are based on the method of successive approximation and allow a choice between parallel and serial readout. Both, the method of conversion and the type of readout, have a decisive influence of the design of the special purpose computer.

First, the choice between parallel and serial readout has to be made. Data can be handled faster in parallel than in serial form at the expense of more complicated circuits. Parallel data transfer from the adaptor to the control unit, requires a great number of lines. Internal connection inside the adaptor are quite numerous when the data presented by the A/D converter to the special purpose computer is in parallel form, and the circuits, which have to perform limit monitoring, are bulky. The speed advantage offered by parallel data processing is diminished when the conversion speed of small A/D converters with adequate resolution is considered. Comparing parallel to serial form makes it apparent that serial form,with its simplicity and inherently higher reliability, is the superior choice.

Acceptance of serial data processing for the adaptor requires a decision as to the direction of data flow. Most A/D converters use the method of successive approximation. Such a

converter produces the most significant bit first. At first glance it seems necessary to reverse the data flow in order to obtain the least significant bit first as required by the arithmetical operations necessary for limit monitoring. A reversible shift register in the A/D converter or data transfer in parallel form from the A/D converter to a buffer shift register, and then shifting out the least significant bit first would accomplish this. Both solutions lead to bulky circuits requiring numerous interconnections.

A close examination of the above problem offered an alternate solution. A two step decision circuit was conceived which allows comparing the measurand to the limits with the most significant bit occuring first. (The theory of this method of comparison is given in the appendix). This circuit is a trifle more complicated than one designed for the least significant bit occurring first, but obviates reversible shift register of buffer register. Data from the A/D converter can be operated on directly in its original direction of flow.

In the above discussion, it was tacitly assumed that limit monitoring is performed in digital form. It is easily conceivable to perform the camparison of the measurand to the amplitude limits in analog form but storage of the limits in analog form without mechanical means is almost impossible. With rate of change limits these difficulties are enhanced.

Limit storage can easily be accomplished in digital form with modern MOS FET integrated shift registers. Such registers

are available with up to 100 places in one package. It was these devices which led to the decision to use MOS FET integrated circuit modules for the entire circuitry of the special purpose computer in preference to bipolar types.

Even with the limits stored in digital form comparison (monitoring) could still be carried out in analog form. The buffer register of the A/D converter could be loaded with the binary equivalent of a limit thereby producing the equivalent analog value at the output of the ladder network of the A/D converter. This output would then be compared to the measurand. The output of the comparator would indicate whether the limit had been exceeded. The signal thus obtained could be used to signal an alarm to the control unit.

The above scheme works well with amplitude limits, but with rate of change limits a more complicated method is required.

The rate of change which is the time derived of the measurand M can be approximated by the change of the measurand within a known time interval divided by the length of the time interval.

$$\frac{dM}{dt} = \frac{M(t_2) - M(t_1)}{t_2 - t_1} = \frac{\Delta M}{\Delta t} \qquad \Delta t = \text{const.}$$

This approximation can be obtained by taking the difference of two samples of the measurand which have been taken a known length of time apart. If the length of time is kept constant for every pair of samples, then the difference is proportional to the rate of change. This - or any similar - method

requires a memory to retain the first sample and an arithmetical circuit that produces the difference. It follows that nothing is gained by analog limit comparison once the limits have been stored in digital form; for the arithmetical operation to obtain the difference requires circuits which are equally complex whether comparison is carried out in analog form by the comparator of the A/D converter or in digital form after conversion. Moreover, an advantage is gained by digital comparison because the A/D converter does not have to change its mode of operation periodically to perform limit comparison there by simplifying synchronization considerably.

The next points to be discussed are intimately connected with the choice of format of one channel word. One channel word is the set of bits which allows the control unit to communicate with one adaptor. Adaptors (channels) from which a signal is desired must be addressed, other channels must be interrogated whether any of the limits has been exceeded or not. Channels where a change of limits is desired must receive the proper command and the time base for rate of change monitoring must be provided. Commands and addresses can be transmitted on one line. It is not possible to send the values of the limits over the same line because of their possible misinterpretation as addresses. Two lines common to all adaptors in the system will suffice to keep commands and limits separate, one the address line and one the limit line.

The adaptor will receive on its address input a continuous flow of addresses. One of these addresses might be its own. Because of the serial nature of these addresses some means must be found to indicate the beginning of an address. It is possible to provide a synchronization signal on a separate line at the beginning of an address. However, this contradicts the requirement for minimum lines between adaptor and control unit. Therefore, a scheme was adapted in which the first bit of each address is a "1". Still, even in this case, erroneous addressing might occur. For, if an address is immediately followed by the next, any "1" could be considered as the beginning of an address. To avoid such a malfunction each address is followed by a number of "0" equal to the number of bits constituting an address. The sampling rate of a system using this scheme is only half of that employing a separate synchronization line, but this can be remedied by dividing the adaptors of the system into two groups each with its own address line. The address on one line then occurs during the "0" on the other line. Depending on the required speed a system with two or one address line can be chosen.

Next, a way must be found in which an alarm condition is reported by the adaptor to the control unit. Using a common line for the alarm signals makes it necessary to establish a time sequence in which the individual adaptors are allowed to send out their alarm signal. If they were to occur at random, several might occur at the same time and identification of the channel in which the alarm occurred would be impossible. The time sequence

is established by doubling the number of bits of one channel word. The first half is then used for signal addressing and the second half for alarm addressing. The alarm addresses are produced by the control unit in a predetermined sequence which does not change during the operation of the system. Each adaptor is interrogated in turn and if it had detected an alarm condition, will send out a signal upon receiving its alarm address. The price at which alarm signal separation is obtained is again a reduction of sampling rate and again this can be remedied by adding a line carrying alarm addresses only. However, because signal and alarm addresses do not occur during the same time interval it becomes possible to send both the information and the alarm signal on the same line.

Disregarding the power lines, one more line is required besides address and signal output lines, the limit line. During limit loading four binary numbers have to be transmitted to a selected adaptor, upper limit, lower limit, positive and negative rate of change. These numbers comprise 10 bits each, (length of one converter word) together 40 bits. If the length of one address word is also chosen 10 bits - which gives an adequate number of addresses - then the channel word will have the same length as one limit word, viz. 40 bits. With limit and channel word of the same length it becomes possible to change limits within one channel word - an advantage when considering the programming of the control unit. One channel word is shown in Fig. 3.1. The first bit of both, the signal and the alarm address word is a "1". The ninth bit of a signal address word is always a "1", while its

tenth bit is normally "0" and becomes a "1" periodically as required to establish the time base for rate of change monitoring. The ninth bit of an alarm address word is always a "0". The tenth bit is normally "0" and is made "1" when it is desired to load limits. Seven bits of an address word are used for addressing proper and allow 127 different addresses to be generated.

As mentioned before the individual adaptors do not contain clocks. The clock is common to all adaptors and is located in the control unit. Pedestal pulses on the address line provide the proper timing for the adaptors. The clock rate is decided by the maximum speed at which the shift register can be safely operated and is 100 kHz.

Fig. 3.2 shows the time relationship between the addresses (signal and alarm) and the signals (output and alarm).

Fig. 3.3 shows a way of increasing the sampling rate with two address lines and one common signal line. One common signal line can be used without the danger of mixing signals.

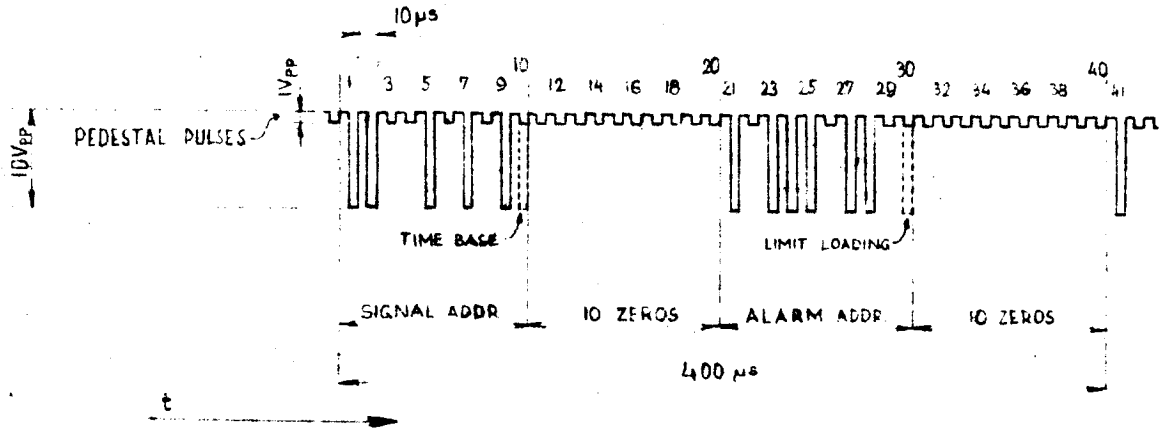


FIG 3.1

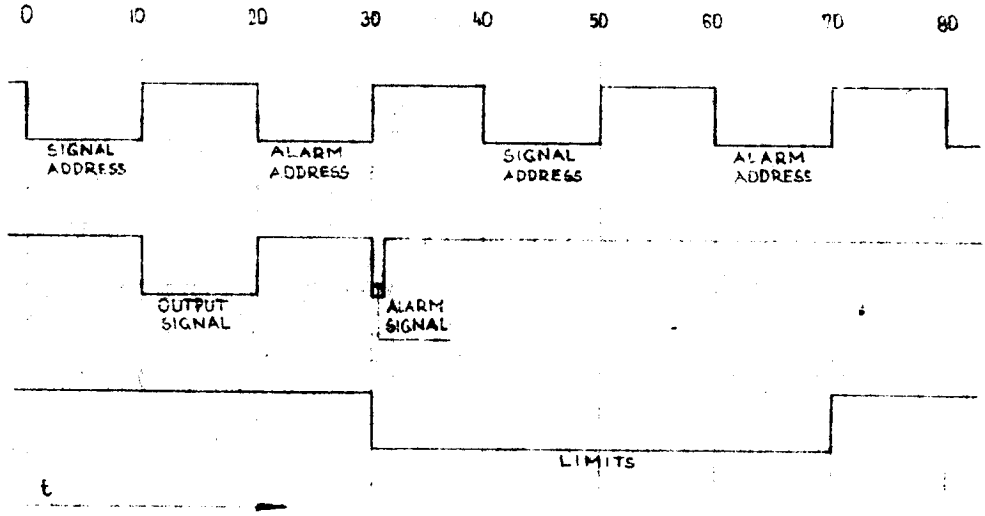


FIG. 3.2

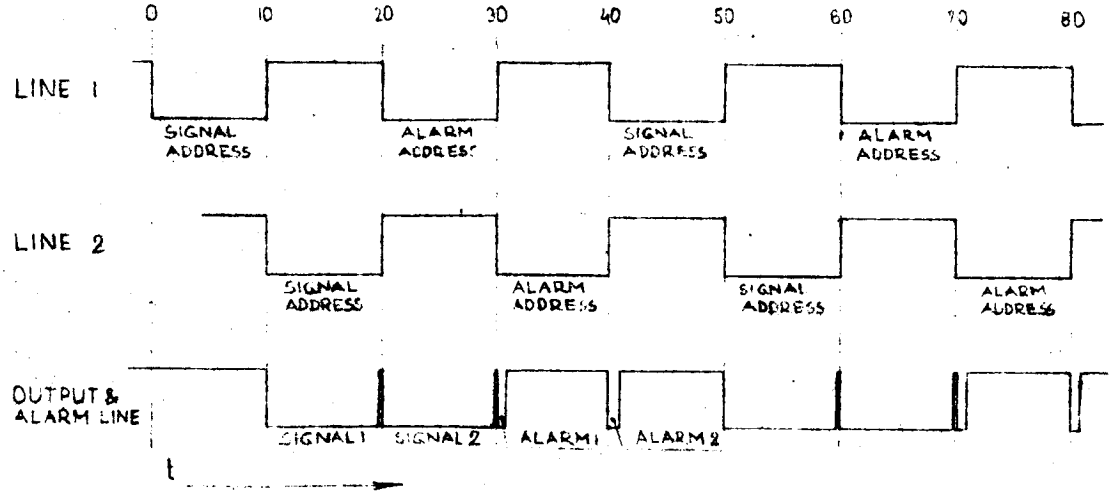


FIG 3.3

4.0 THE DIGITAL ADAPTOR MODULE

4.1 Functional Description:

The digital adaptor is intended to be used in multichannel data acquisition system. It receives commands from and sends signals to a command unit as shown in Fig. 4.1. All adaptors share the same communication lines. Only three such lines are necessary: Address line, limit line and signal line.

The address line carries coded address signals allowing to interrogate any channel and also synchronization pulse to assure proper timing of the internal operation of each adaptor.

The limit line transmits a set of limits to a adaptor which is selected to receive this set by a command on the address line.

The signal line transmits a signal from any adaptor which has been addressed. This signal can be an output signal corresponding to a transducer output or an alarm signal indicating that the limits in the addressed channel (adaptor) have been exceeded.

Block diagram Fig. 4.2 shows the major functional blocks of one adaptor module. Also shown is the manual limit setting box, which makes it possible to adjust individual channels locally.

A signal on the address line is entered into the address register and decoded. These signals on the address line are sent out in groups called "channel words". Fig. 3.1 shows the format of such a channel word. It consists of four groups of 10 bits each. The first 10 bits contain the signal output address (bits 2 through 8), a bit indicating the beginning of an address word. (bit 1) a bit indicating that the address received is a signal

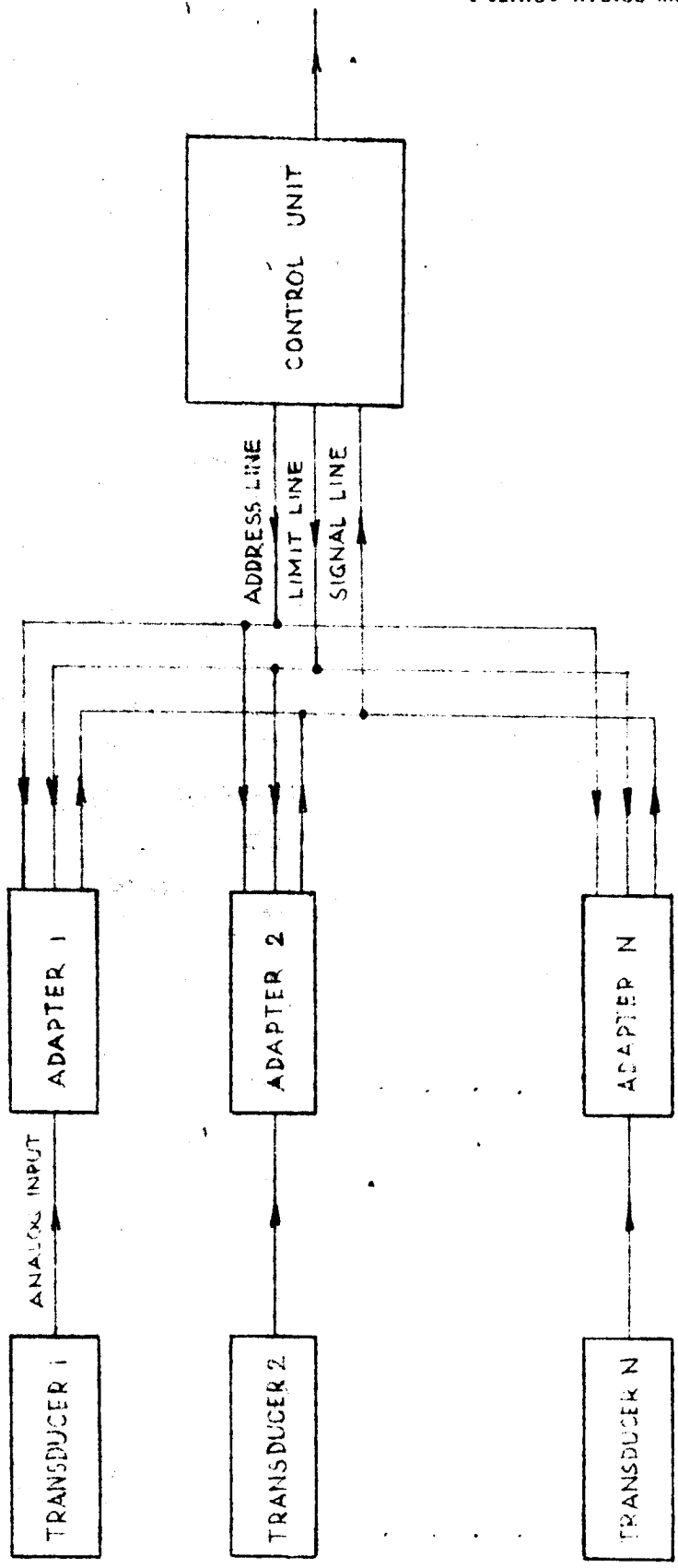

CONTROL UNIT
ADDRESS LINE
LIMIT LINE
SIGNAL LINE
ADAPTER 1
ADAPTER 2
ADAPTER N
ANALOG INPUT
TRANSDUCER 1
TRANSDUCER 2
TRANSDUCER N

FIG.4.1

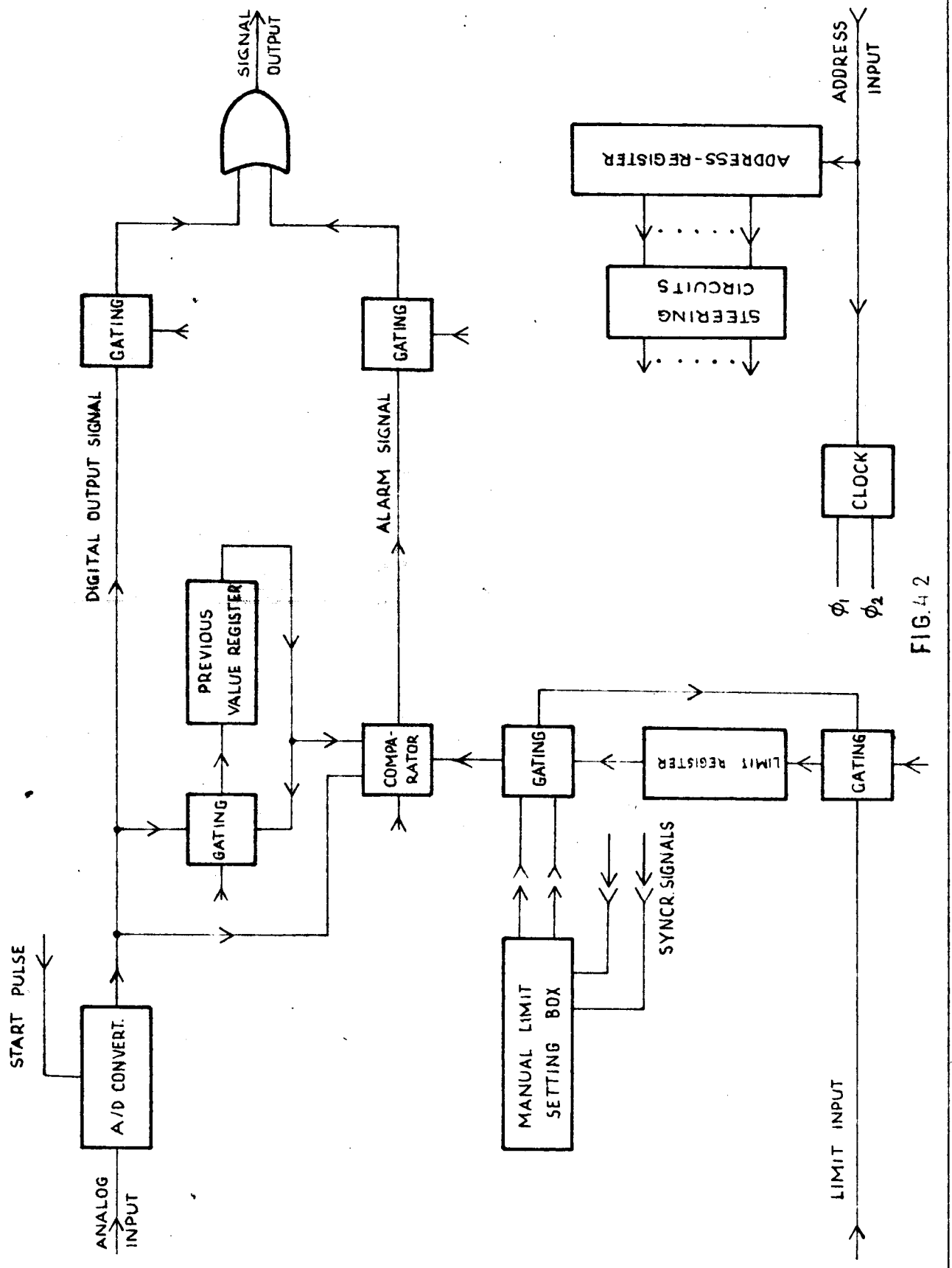

SIGNAL OUTPUT
ADDRESS INPUT
ADDRESS-REGISTER
STEERING CIRCUITS
GATING
GATING
DIGITAL OUTPUT SIGNAL
ALARM SIGNAL
CLOCK
ϕ_1
ϕ_2
PREVIOUS VALUE REGISTER
GATING
COMPA-RATOR
GATING
LIMIT REGISTER
GATING
START PULSE
A/D CONVERT.
MANUAL LIMIT SETTING BOX
SYNCR. SIGNALS
ANALOG INPUT
LIMIT INPUT

FIG. 4.2

output address (bit 9) and a bit establishing the time base for rate of change monitoring (bit 10). Bit 10 is not contained in every address word but occurs only at certain times as dictated by the selected time base. The second group is ten zeros which allow the address register to clear and prevent erroneous addressing, for if one address were followed immediately by the next or spaced fewer than 10 bits, then any "1" followed by a combination of "1's" and "0's" could be considered an address and be recognized as such by an adaptor.

The third group of ten bits contains the alarm output address (bits 2 through 8), a bit indicating the beginning of an address word (bit 21). Bit 9 is "0" indicating that an alarm output address has been received and bit 10 is "1" whenever limit loading is desired.

The following ten bits are again all "0's" for the same reason as the bits following the output address.

The adaptor can be operated in four different modes: 1) silent mode, 2) active mode, 3) alarm mode, 4) limit loading mode.

When in the silent mode the adaptor is not addressed. It therefore sends out neither an output signal nor an alarm signal. However, it does receive timing and command signal by the presence or absence of the bits 1, 9, 10, 21, 29, and 30. These signals are decoded and control A/D conversion, and limit monitoring. During the silent mode the limits are shifted out of the limit storage register, re-circulated and periodically changed upon a command by the control unit (bits 1, 9, and 10 of the received

address are "1's").

The adaptor is placed in the active mode by receiving its own signal address (bit 9 is "1"). 10 bits representing the digital equivalent of the measurand are then sent out on the signal line.

The adaptor is in the alarm mode when any of the limits has been exceeded (a "1" has been stored in the comparator) and it has received its own address. The "1" stored in the comparator will then be sent out on the signal line.

The adaptor is placed into the limit loading mode by receiving its own alarm address with bit 10 being a "1". Recirculation of the contents of the limit storage register is interrupted and the limit input opened to accept a new set of limits from the control unit.

The limits stored in the adaptor can also be changed manually by means of an auxiliary circuit contained in the manual limit setting box. Upon command the manual limit setting box interrupts the recirculation of the stored limits and shifts a new set of limits into the limit storage register. Proper synchronization of the shifting process is assured by synchronization signals picked up by the manual limit setting box from the adaptor.

4.2 Timing of Events:

The detailed functioning of the adaptor is described in the time tables 1 through 4, Appendix B. The wave forms at important points inside the adaptor are shown in Fig. B.1 through B.4, Appendix B. The logic block diagram Fig. 4.3 complements the information contained in the time tables and wave shapes.

The time tables, the wave shapes and the logic block dia-

gram are based on the following assumptions:

1) The signal address of the adaptor module is 1000111110 and the alarm address is 1000111100.

2) In all modes with the exception of the silent mode the module has received its own address.

3) The limits stored in the module during all modes with the exception of the alarm mode are:

Current value C (output of A/D converter) is 1100000110.

Previous value P is 1010000101.

Upper limit UL is 1100000111.

Lower limit LL is 1000000001 and its 1's complement $\overline{LL}$ is 0111111110.

Δ^+ is 0010000110.

Δ^- is 0100000110.

4) Current value C during alarm mode is 1110000110.

4.3 Detailed Circuit Description:

A few more words are necessary for the understanding of the functioning of the decoder (registers SR 4 and SR 5 and gates OR 7, OR 8, and A 9, Fig. 4.3), the limit storage register with its steering gates (register SR 1, gates OR 5, OR 6, OR 10, OR 11, A 4 and A 15, Fig. 4.3), the previous value register with its steering gates (register SR 2, gates OR 1, OR 1 and A 1, Fig. 4.3) and the pulse shaper (see schematic diagram, Transistors Q 4 and Q 5).

4.3.1 The Address Decoder:

An address word appearing on the address line is entered into SR 4 and its one's complement obtained from inverter I 1 is entered into SR 5. The states of the outputs of SR 4 after 10 steps when the first bit of the address word (which is always a "1") appears at output 1 of SR 4 indicating that an address has been received. The other outputs of SR 4 have now assumed states which correspond to the address word while the states of the outputs of SR 5 correspond to the one's complement of the address. Two NOR gates are used to decode the state of the registers. NOR gates OR 7 and OR 8 will become both "1" when all their inputs are "0". Consequently, the outputs of SR 4 which correspond to "0's" of the address and the outputs of SR 5 which correspond to "1's" of the address are connected to the inputs of the NOR gates OR 7 and OR 8. Seven bits of each address word are available for identifying one channel while the remaining three serve for synchronization and mode control. The decoding matrix shown in the logic block diagram Fig.4.3 is wired for the signal address 1000111110 and the alarm address 1000111100. When OR 7 and OR 8 are both "1", A 9 is also "1". The output of A 9 by itself has no effect on the module unless one of the gates A 10, A 11, or A 12 are also "1" at the same time.

Decoding could have been done by using one or more AND gates in place of the NOR gates. However, available circuit modules dictated the approach using NOR gates.

4.3.2 The Limit Storage Register:

The limit storage register SR 1 is connected to two arrangements of gates. These gates control recirculation and limit loading. When the limits are recirculated the outputs of the gates OR 5 and OR 10 are kept "1" by making one of their inputs "1". Signals on their other inputs will not change their outputs. The output of SR 1 can pass OR 11 because its second input is kept at "0" and then inverted by A 15 whose second input is "1" as long as OR 10 is "1". The inverted contents of SR 1 then reach OR 6 whose second input is kept at "0" and therefore passes the sign 1 to A 4. The second input of A 4 is "1" because of OR 5 being "1". The signal can pass A 4, is inverted by it and re-enter into SR 1 in its original form.

During limit loading when a signal appearing on the limit line is entered into SR 1 and flip flop FF 3 had changed states, OR 6 is kept at "1" thereby blocking recirculation. The second input of OR 5 is now "0" and the signal on the limit line is free to pass to be entered in inverted form into SR 1.

During manual limit loading when a set of limits is to be entered from the limit loading box, OR 5 and OR 6 remain in the same state as during recirculation, OR 11 is now kept at "1" and OR 10 allows the signal to pass. However, because of the double inversion by A 15 and A 4, the limits must be applied to OR 10 as their one's complements. The manual limit loading box is wired in such a manner, that the limits entered into its registers are in inverted form.

4.3.3 The Previous Value SR 2 Register:

The previous value register must provide to the comparator gates the following periodic sequence: previous value, 10 "0's", one's complement of previous value, and 10 '0's". This sequence is produced by taking advantage of the inverting property of the gate arrangement OR 1, OR 2 and A 1.

When the output of the A/D converter is transferred to SR 2, OR 2 is "1" while the second input of OR 1 is "0". (see Time Table 1). A 1 inverts the signal and places it into SR 2. OR 1 is then kept at "1" by the $\overline{Q}$ output of RG 4 until the time base signal arrives. OR 2 is also kept at "1" for the next 10 clock pulses. The output of A 1 is "0" and 10 "0's" are placed into SR 2. Following these 10 "0's" the complement of the previous value is shifted out of SR 2. The second input of OR 2 is now "0", the signal can pass and is inverted by A 1 and is entered into SR 2. OR 2 then goes to "1" again and 10 "0's" are shifted into and out of SR 2. After these 10 "0's" the previous value in its normal form appears at the output of SR 2 and one recirculation corresponding to one limit comparison cycle is completed.

4.3.4 The Pulse Shaper:

The pulse shaper provides the necessary clockpulses for the adaptor. Its two outputs are the complements of each other. Pulses greater than -1V received on its input will saturate Q 5 so that the pedestal pulses on the address line are sufficient to produce a 0 to -10V signal at the collector of Q 5. This signal is then inverted by Q 4. The signal at the collector of Q 5

corresponds to clock pulses ϕ_1 and the signal at the collector of Q 4 corresponds to clock pulses ϕ_2.

4.4 Implementation:

4.4.1 Components:

The largest single item required for the implementation of the digital adaptor transducers is the A/D converter. The only unit on the market which meets both, the size and the cost requirement is Pastoriza Electronics" A/D converter Model ADC-10_{IC}. The interface circuits for integration of the converter with the other circuits are simple: only three level changers are necessary (serial output, start pulse and clock pulse). The only modification required will effect the serial output which in this application will be taken from a different point than in the standard model. Appendix G is the schematic diagram of Pastoriza Electronics' A/D converter with the intended changes entered upon it. The performance specifications of the A/D converter, Appendix H, will also govern the performance of the adaptor module.

The logic circuits which perform limit storage, limit comparison and decoding will be implemented by MOS field effect transistor integrated circuit module produced by General Instruments and the MicroElectronics Division of Philco. It was attempted to keep the number of different modules to a minimum and, therefore, extended use was made of Philco's module pL4G01. This module contains 2 gate arrangements with 4 inputs each. By interconnecting the terminals of this gate arrangement a large variety of logic function can be produced. In the adaptor this module

is used as register, AND gate, NAND gate, OR gate, NOR gate and inverter.

Other very useful devices are General Instruments' shift registers MEM 3021 and MEM 3012 SP. These devices which come in packages no larger than a flip flop and have a capacity of 21 and 12 bits, respectively, made it possible to keep size and power consumption of the adaptor within realistic limits.

Another significant saving in size could be realized by taking advantage of the logic functions of Philco's decoder pL4G02. This one module performs the functions of the 4 AND gate A 10, A 11, A 12 and A 13 (see Logic Diagram, Fig. 4.[illegible]).

The complicated majority function (gate M) required for limit comparison is obtained from the carry output of a full General Instrument's full adder MEM 1000. The second full adder contained in this module is used as an exclusive OR gate (OE 1).

OR gate, OR 12, is not an integrated circuit module but consists of two diodes. These two diodes not only act as an OR gate but also prevent signal on the signal line from entering the adaptor.

A few circuit functions cannot be implemented by integrated circuit modules. These are the level changers (Q 1, Q 2, and Q 3) and the pulse shaper (Q 4 and Q 5, Schematic Diagram). The transistors chosen for this task are well proven types available as military versions.

The complete Parts List can be found in Appendix E.

4.2.2 Packaging:

The chosen packaging approach was influenced by the following consideration:

1) Design and development of the adaptor module will only be carried out to the prototype stage.
2) While a prototype in nature, the packaged adaptor must be small enough to demonstrate its usefulness and show promise of future size reduction.
3) The packaging method must be flexible enough to allow changes when necessary.
4) The packaging method must be inexpensive considering the small quantities involved.

The packaging method adopted for the job is deemed to be a good compromise between manual and machine work.

The basic idea of this approach is the same as the one used by Engineered Electronics Co. in their Microstick System.

The integrated circuit packages are mounted on several layers of conductor patterns separated by insulating layers. Fig. 4.8 shows an exploded view of such an arrangement.

Because of the many different conductor layers required a way had to be found to produce them as efficiently as possible. The adopted approach starts with a basic conductor pattern shown in Fig. 4.9. Of this pattern as many negatives are made as there are different conductor patterns. Unwanted conductor pattern is then blanked out (see Fig. 4.9). From the negatives thus obtained the conductors are made from two-ounce

$$\sum_{h=1}^{d} A_h\, 2^{h-1} - \sum_{h=1}^{d} (B_h + C_h)\, 2^{h-1} \geq 2 \qquad (10)$$

$$\sum_{h=1}^{d} A_h\, 2^{h-1} > \sum_{h=1}^{d} (B_h + C_h)\, 2^{h-1} \qquad \text{q. e. d.}$$

4.) $A \gtrless B + C$

if $A_d > B_d + C_d$ or $A_d = 1,\ B_d = C_d = 0$ (3)

$B_j + C_j = A_j + 1$ or $A_j = B_j = 0,\ C_j = 1$

$A_j = C_j = 0,\ B_j = 1$ (4)

$j = g + 1, \ldots, d-1$ $A_j = B_j = C_j = 1$

$A_g + 1 < B_g + C_g$ or $A_g = 0,\ B_g = C_g = 1$ (11)

from (7): $$\sum_{j=g+1}^{d} A_j\, 2^{j-1} - \sum_{j=g+1}^{d} (B_j + C_j) 2^{j-1} = 2^g \qquad (12)$$

from (11): $$A_g\, 2^{g-1} - (B_g + C_g)\, 2^{g-1} = -\, 2^g \qquad (13)$$

adding (12) and (13) $$\sum_{j=g}^{d} A_j\, 2^{j-1} - \sum_{j=g}^{d} (B_j + C_j)\, 2^{j-1} = 0$$

$$\sum_{j=g}^{d} A_j\, 2^{j-1} = \sum_{j=g}^{d} (B_j + C_j)$$

The first $d + 1 - g$ bits are not decisive and it is necessary to look at the remaining bits 1 to $g - 1$ for a condition $A_i \neq B_d + C_d$.

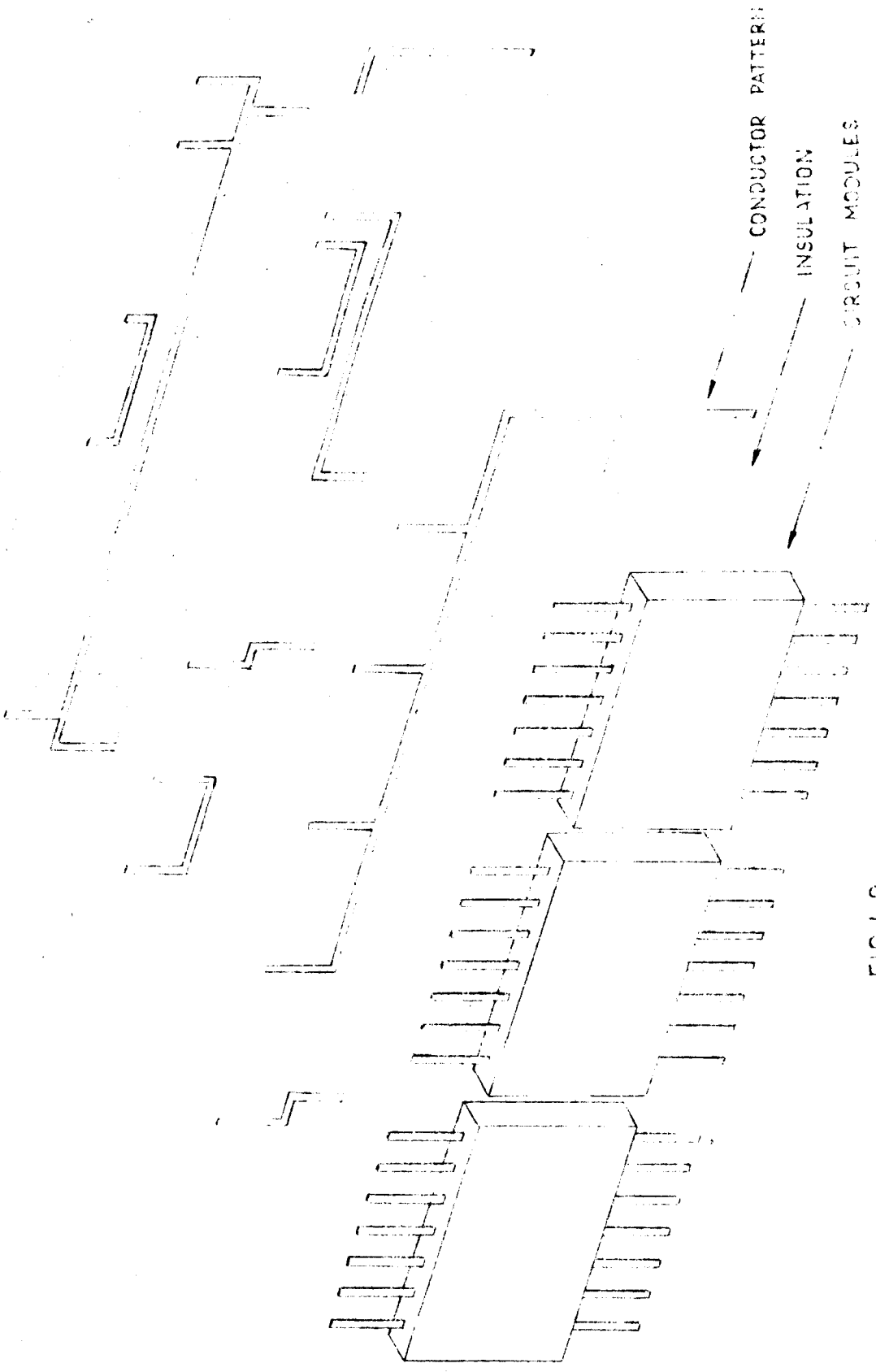


FIG.4.9

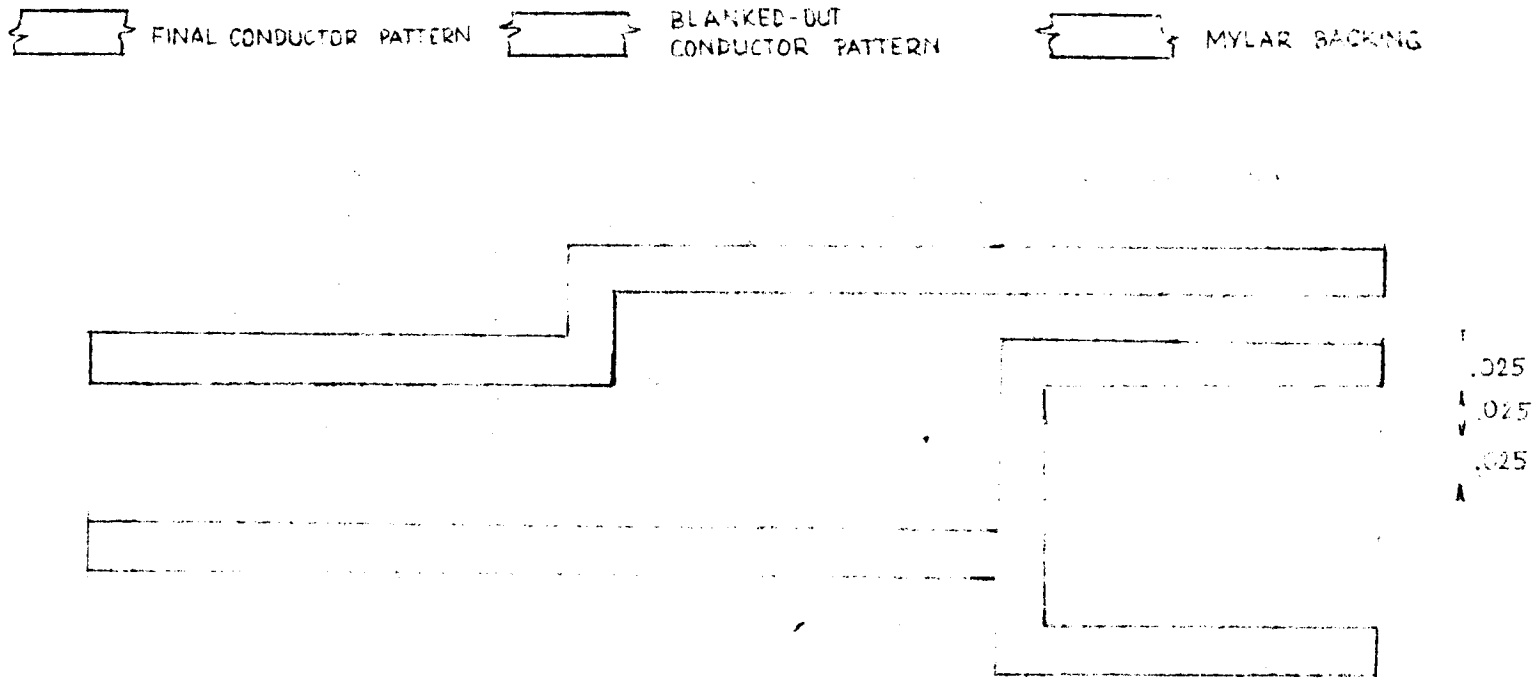

FINAL CONDUCTOR PATTERN
BLANKED-OUT CONDUCTOR PATTERN
MYLAR BACKING
.025
.025
.025

FIG.4.9

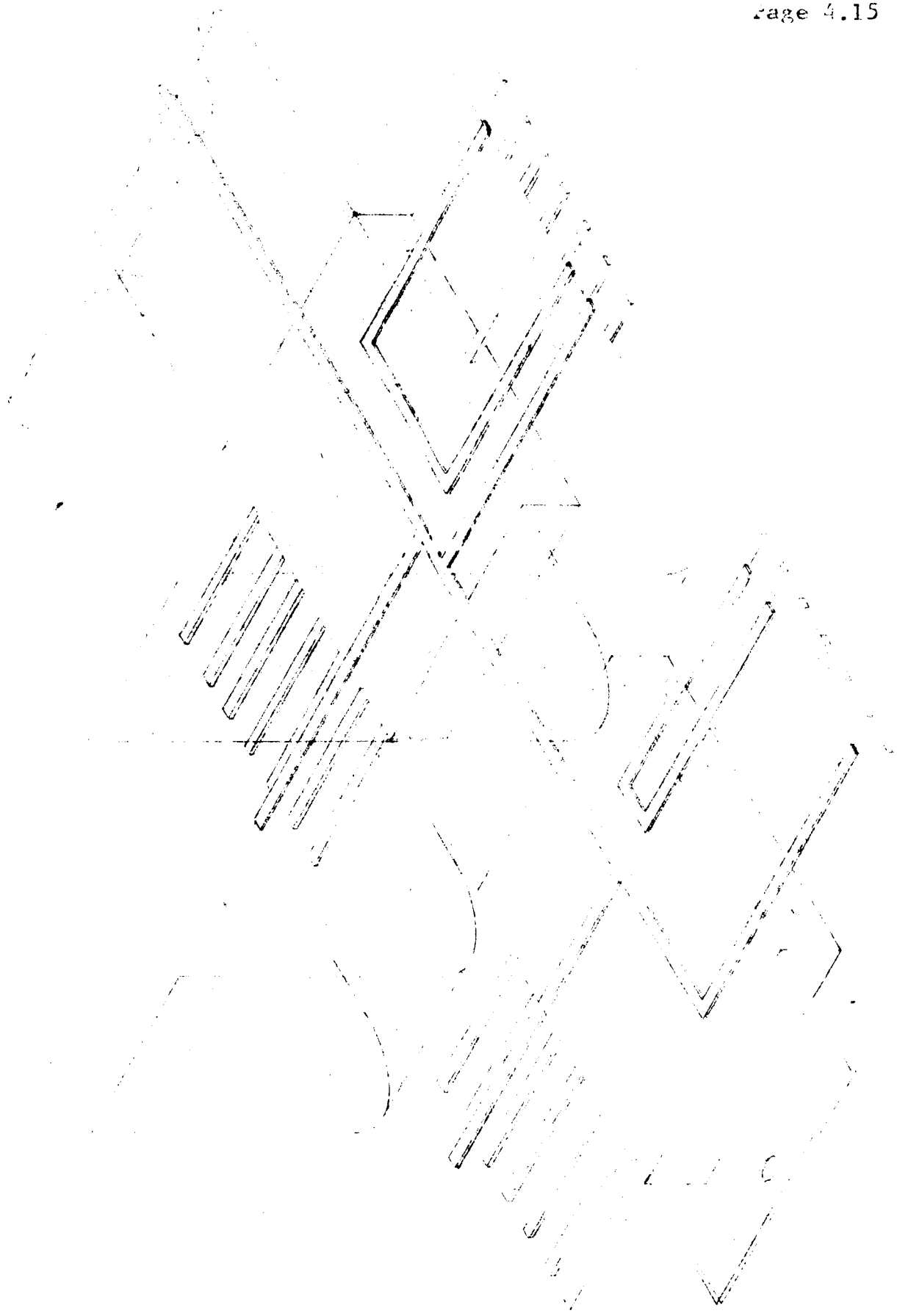


FIG 4.5

1. A/D CONVERTER
2. MOTHER BOARD
3. PATCH-BOARD CONNECTOR
4. CIRCUIT MODULES
5. CONNECTOR FOR LIMIT LOADING BOX
6. PLUG-IN CONNECTOR

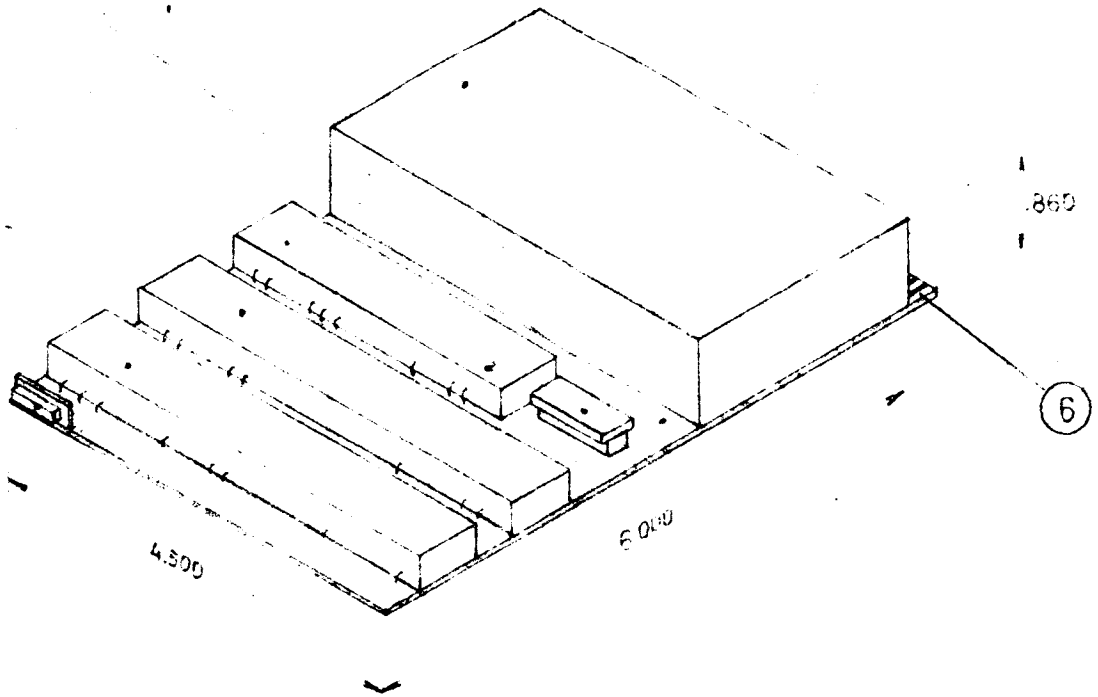


FIG.4.11

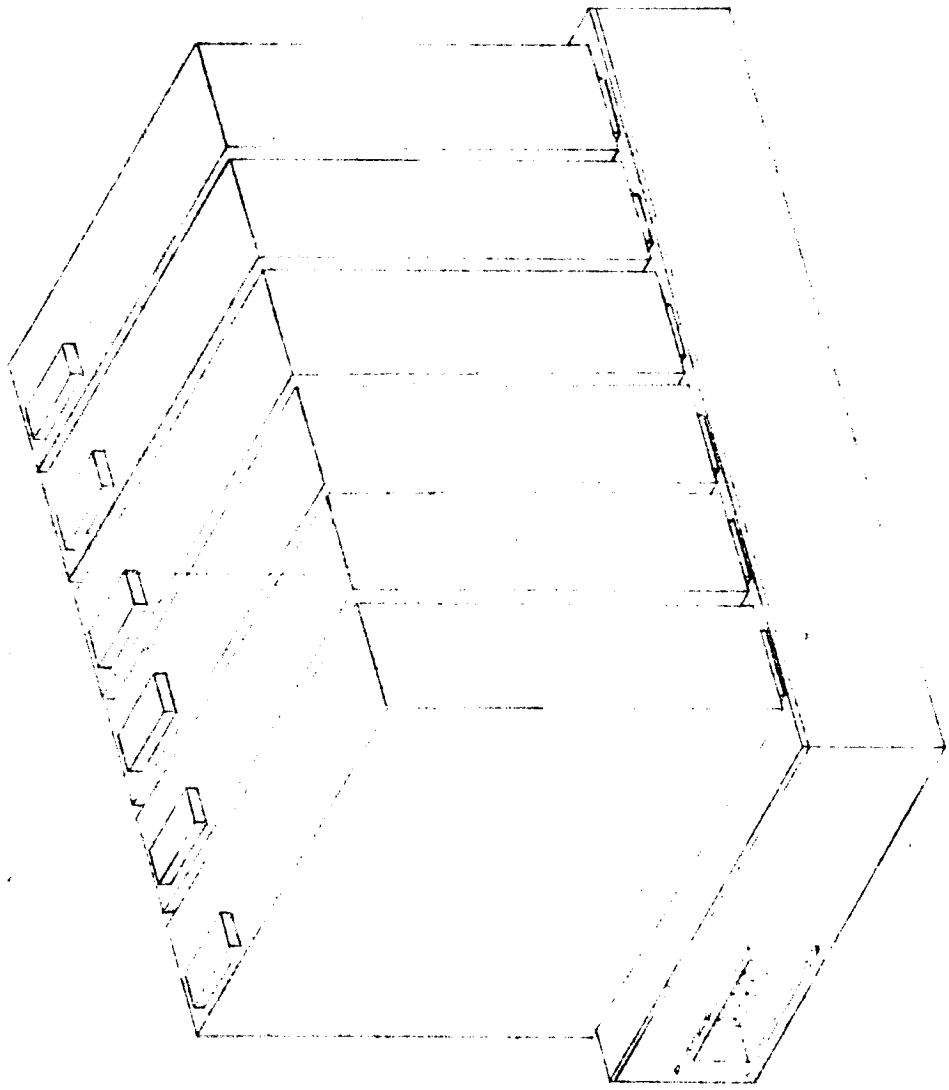


FIG.4.12.

copper foil backed with adhesive Mylar by standard etching techniques.

For assembly the circuit packages are placed into a jig and the conductor layers soldered into place. Before the soldering takes place part of the Mylar backing covering the comb-like leads of the conductor pattern is removed to allow soldering to the circuit modules. (see Fig. 4.10) After soldering the circuit packages are potted to give them sufficient structural strength.

The 30 integrated circuit modules of the logic part of the adaptor can be packaged in only three units. The finished packages are then mounted on the mother board (Fig. 4.11) which also carries the A/D converter. Each adaptor is equipped with a ITT Cannon-Micro D MDB1-25 connector which has its counterpart on a chassis (Fig. 4.12) which accepts the 6 adaptors of the complete system.

5.0 MANUAL LIMIT LOADING

5.1 Circuit Description:

The limits stored in the adaptor can be replaced by a new set either automatically by the control unit or manually by the so called manual limit loading box. This box can be connected to any of the adaptors whose set of limits is to be changed. Fig. 5.1 shows the logic block diagram of the manual limit loading box. It picks up power and synchronizing signals from the adaptor through a connector. The limits are entered into the box in binary form. The lower limit is entered as its 1's complement. The sequence is Δ^- (negative rate of change), lower limit, Δ^+ (positive rate of change) and upper limit.

The limits are first entered into register SR 10 by closing the switches S 0 through S 15 which correspond to "1"s. The switches are connected to the direct reset inputs of the register stages. In this manner the one's complement of the word being entered is contained in the register.

After a limit has been entered into SR 10 it is shifted into SR 40 by closing S 3. The $\overline{S}$ input of FF 1 is then "0" and the first pulse from CL of the adaptor sets FF 1 to "1". CL 1 is "1" while at the output of CL 2 clock pulses appears. The clock pulses are inverted by L 1 and correspond now to clock pulses 2. The contents of register SR 10 are shifted into SR 40. After 10 clock pulses a second pulse from CL 2 of the adaptor arrives at the trigger input of FF 1 and resets it. SR 10 is now ready to accept the next limit.

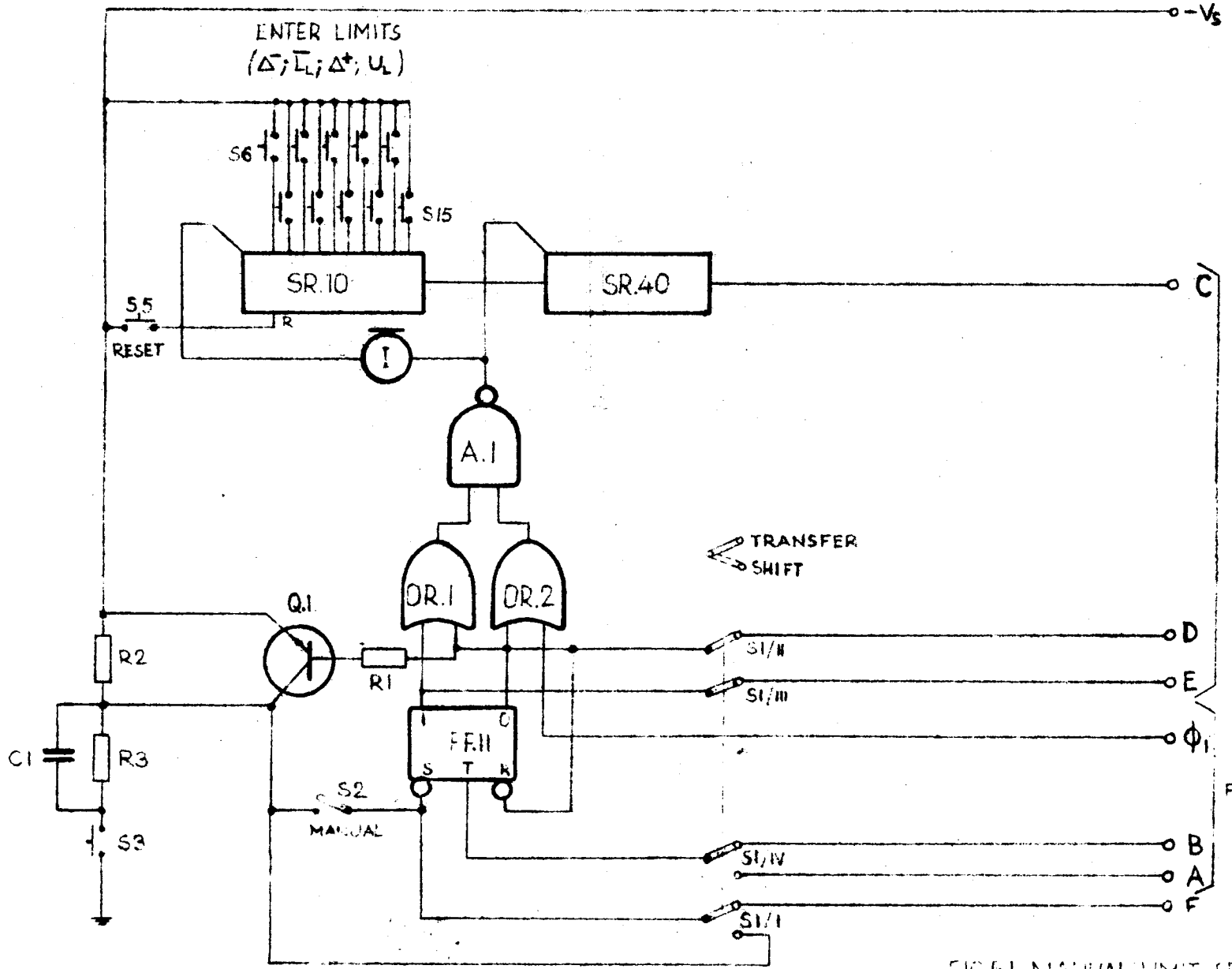


FIG.5.1 MANUAL LIMIT SETTING BOX

Transistor Q 1 makes sure the $\bar{S}$ input of FF 1 is returned to $-V_{DD}$ the moment FF 1 goes into its "1" state. A second setting of FF 1 thereby avoided as long as S 3 has not been opened again long enough to allow C 1 to discharge.

After 4 limits have been shifted into SR 40 it is now possible to transfer these values into the limit storage register of the adaptor. S 1 is set into the transfer position and upon closing of S 3 and triggering of FF 1 by the first pulse from the "1" output of FF 5 of the adaptor. OR 11 of the adaptor is kept at a "1" blocking the contents of the limit register of the adaptor from recirculation, while the new limits from SR 40 can pass through OR 10 and A 15 to the input of the limit register of the adaptor.

5.2 Implementation:

The same type of MOS field effect transistor integrated circuit modules will be used for the manual limit setting box as for the adaptor.

The packaging requirements for this circuit are not so stringent as for the adaptor. The volume taken up by the circuits is small in comparison to the switches for limit entering. The integrated circuit modules will be mounted in sockets and the interconnections will be made with wires. The circuits will be encased in a standard aluminum case measuring 6½ x 3½"x 2½" fitted with a cable for connecting to the adaptor.

The complete Parts List can be found in Appendix E.

6.0 CONTROL UNIT FOR TESTING

During the testing of the proposed system of 6 adaptors it will be necessary to provide synchronization, to generate addresses, to display the output signals and load the limits. These functions which will ultimately be performed by a specially programmed computer are indispensable for the operation and check out of the system.

The control unit for testing must be inexpensive and, therefore, simple. It is the address generating circuits where the most significant savings can be obtained. Rather than attempt to generate all 127 possible addresses in any desired sequence, the address generator is limited to 6 addresses in one sequence. The display for the output signal is also kept to a minimum. Only one channel can be displayed at a time. To display more than one channel at the same time would add nothing to the usefulness of the test set-up for, only one channel can be evaluated at a time.

6.1 Circuit Description:

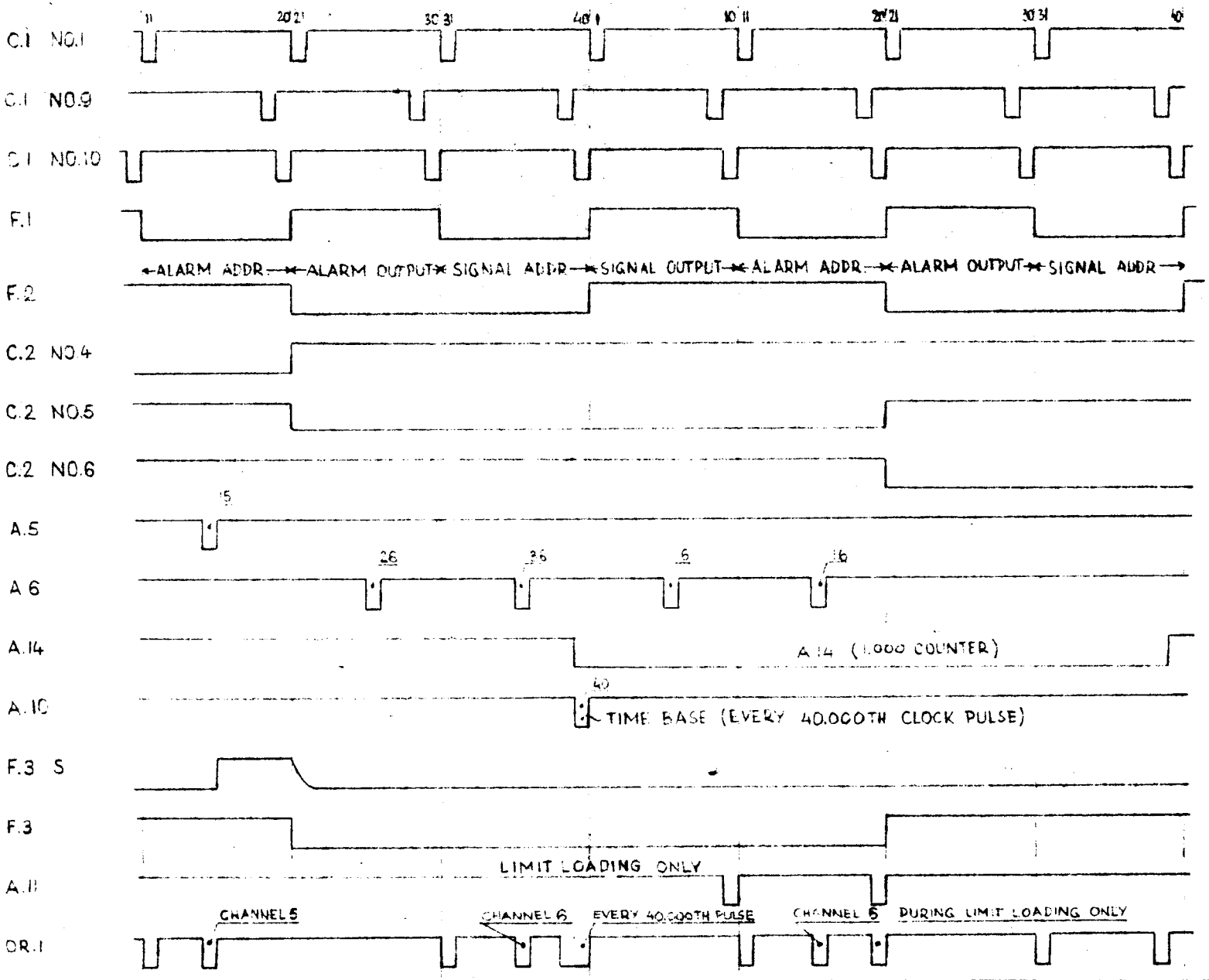
Fig. 6.1 shows the block diagram of the control unit. An external pulse generator serves as a clock. Clock pulses of both phases, ϕ_1 and ϕ_2 are available at a rate of 100,000 pulses per second. Counter C 1 is counting at this rate and each of its 10 outputs becomes "1" every 10th clock pulse. Output 1 triggers flip flop FF 1 causing it to change states every 10 pulses. The "1" output of FF 1 in turn triggers FF 2 which changes states every 20 clock pulses. In this manner, the basic interval of 10 "0's" of a channel word which alternate with signal and alarm addresses are obtained by alternately blocking OR 1 by the "0"

output of FF 1. The inverted output of OR 1 stays at "0" as long as FF 1 is in its "0" state. The "1" output of FF 2 is a square wave with a period of 40 clock pulses corresponding to the length of one channel word. The "1" output of FF 2 is applied to counter C 2 which is therefore advanced by one count at the beginning of each channel word. (See wave shapes Fig. 6.2) C 1 is a module 8 counter and its outputs are connected to AND gates A 2 through A 7. Any one of these gates will be enabled for 40 pulses if its inverted input is returned to zero through the switch connected to it. The output of such a gate will then be a "1" when the output of C 1, to which it is connected, becomes "1", that is four times during one channel word. Only two of these signals, spaced 20 pulses apart, reach the output because CR 1 is blocked every other 10 pulses. Addresses thus produced consist of a single "1" (disregarding bit 1, 9, and 10 which serve to convey commands) positioned in front of or between "0's". Signal and alarm addresses sent out during the same channel word are always the same with the exception of bit 9 which appears in signal addresses only.

By switching any of the switches S 2 through S 7 to the "1" output of FF 1 it is possible to disable the corresponding AND gate during the first 20 bits of a channel word. No signal address is produced in this case, only the alarm address.

Bit 9 used to signify a signal output address must appear only during the first 10 bits of a channel word. Output 9 of C 1 is, therefore, applied to A 9 which is enabled when FF 1 and

FIG.6.2 CONTROL UNIT, WAVE SHAPES.



FF 2 are both in the "1" state (see wave shapes, Fig. 6.2).

Switch S 8 allows selecting the channel to be displayed. During the time C 2 stays in the state selected by S 8, A 15 is enabled. When FF 1 and FF 2 go both to "0" and the inverted output of OR 4 becomes "1" then A 15 passes clock pulses to shift register SR 1. The pulses appearing on the output line of the adaptors are then shifted into SR 1. After 10 pulses FF 1 goes to "1" and A 15 is disabled. For the following 30 clock pulses the contents of SR 1 remain unchanged. During the same period the output of A 16 is "0" and power is applied to the lights B 1 through B 10 through Q 4. Those lights which correspond to a "1" in SR 1 are turned on. When both FF 1 and FF 2 are in the "0" state the period during which SR 1 is loaded and the states of the outputs of SR 1 are changing - all lights are turned off. If the lights were left on, no clear read out could be obtained for lights corresponding to "0's" would also be turned on during loading of SR 1 and glow at various levels of brightness.

Counter C 3 counts the output pulses of A 9, C 3 has a maximum count of 1000 and consists of three module 10 counters. A 9 becomes "1" only once every 40 clock pulses. Consequently, it takes 40,000 clock pulses to complete one revolution of C 3. The decoding network A 12, A 13, and A 14 produces a "1" for 40 clock pulses with a periodicity of 40,000 clock pulses. Its output is applied to A 10 which puts out a "1" when output 10 of C 1 and FF 2 are also "1". This event always takes place on the clock pulse immediately following an output from A 9 there-

by making the output of A 10 part of the signal address. When such an address is received by an adaptor it replaces the previous value stored in the previous value register by the current value. In this manner, the time base for rate of change detection is established. The time base in this case is .4 sec rather than 1 sec which will eventually be used when the system will be controlled by a computer. The shorter time base of .4 sec was chosen to simplify the design and cost of the control unti for testing.

For remote limit loading the manual limit loading box must be connected to the control unit. The limits are placed into the box in the same way as when it is used for loading individual adaptors locally. However, the transfer of the limits from the box to the adaptor is now initiated by closing switch S 1 of the control unit. Closing S 1 forces the inverted set input of FF 3 to "0" and when the output of C 2 (selected by S8) which corresponds to the channel whose limits are to be changed goes to "1" FF 3 is set to "1". A 11 is now enabled and when FF 2 goes to "0" output 10 of C 1 will appear at its output. The inverted output of A 11 is applied to the set input of FF 1 of the limit loading box. This flip flop will go to "1" upon receiving a pulse on its trigger input from FF 2. Clock pulses can now reach the registers of the limit loading box and the limits are shifted out on the limit line. FF 3 is reset by the next "1" from FF 2. FF 1 of the limit loading box is reset 40 clock pulses later when FF 2 goes to "1" again. Limit loading

is then completed.

No provision are made in the control unit to display an alarm signal that might be produced by an adaptor whose limits have been exceeded. Alarm signals are detected on the signal line by monitoring it by an Oscilloscope.

6.2 Implementation:

The control unit employs the same type of integrated circuits as the adaptor.

The control unit for testing is intended for checkout of the adaptor during and after assembly at the factory and is, therefore, of temporary usefulness only. It should be constructed at the lease possible costs. Simple breadboarding with the integrated circuits mounted in sockets will be adequate for this purpose.

The complete Parts Lists can be found in Appendix C.

7.0 SPECIFICATIONS

Performance of the digital adaptor for transducers will conform to the following specifications:

Analog Signal Input

Input Voltage	0 to -10 V
Input Impedance	2.4 kΩ

Digital Signal Output

Word Format	10 bits, non-return-to-zero, most significant bit first.
Resolution	10 mV
Bit Rate	100,000 bits per sec.
Logic Levels	"0" corresponds to 0 V "1" corresponds to -10 V
Word Rate	2,500 words per sec.
Output Impedance	2 kΩ

Limit Input

Word Format	40 bits corresponding to the 4 limits, return-to-zero or non-return-to-zero.
Bit Rate	100,000 bits per sec.
Logic Levels	"0" corresponds to 0 V "1" corresponds to -10 V
Input Impedance	> 5 MΩ

Address Signal Input

Word Format	40 bits allocated to one channel, return-to-zero, pedestal pulses for synchronization.
Bit Rate	100,000 bits per sec.
Logic Levels	"0" corresponds to 0V "1" corresponds to -10 V
Channel Word Rate	2,500 words per second max.
Input Impedance	36 kΩ

Power Requirements

+15 VDC, ± 1%, 20 mA

+ 4 VDC, ± 5%, 300 mA

-13 VDC ± 2%, 85 mA

-26 VDC ± 3%, 65 mA

8.0 TEST METHODS

Realistic testing requires that the adaptor be operated under conditions which resemble those of its eventual application as closely as possible. For this reason a control unit will be constructed which will allow operation of a system of 6 adaptors. The control unit is described in Section 6.0. It provides all synchronization signals, generates addresses and displays the output signal of one channel.

The parameters to be tested can be divided into two groups:

1) Parameters depending on the performance of the A/D converter.
2) Parameters depending on the performance of the logic circuits.

To the first group belong linearity and conversion accuracy which can easily be tested by applying a series of known voltages to the input and comparing them to the values read out at the display of the control unit. This task is equivalent to testing the A/D converter.

To the second group belong address discrimination, pulse shapes, and the accuracy with which amplitude and rate of change limits can be monitored.

Address discrimination and pulse shapes can easily be monitored and checked on the screen of an oscilloscope.

The rise and fall time of the pulses constituting the output signal must be sufficiently short to allow the pulses to assume the correct logic levels of "0" and "1" within one clock time.

Address discrimination can be checked by monitoring the signal output line of the system. If the addresses generated by the control unit do not correspond to any address of the adaptor of the system (for instance, bits 2 through 8 equal to "0", see Fig. 3.1) then no output signal must appear in the time slots of 10 bits immediately following the signal address words.

Testing limit monitoring requires a more eleaborate test set up. Fig. 8.1 shows such a setup for testing amplitude limit monitoring. Fig. 8.2 shows the time relationships of the pertinent wave shapes. The signal applied to the adaptor under test consists of a DC voltage on which a rectangular pulse is superimposed. When the upper amplitude limit is to be tested then the peak-to-peak voltage of the rectangular pulse is adjusted to such a magnitude that the composite signal (DC bias plus pulse) exceeds the upper limit stored in the adaptor. During the time period of 30 clock pulses following the leading edge of the rectangular pulse both, lower and upper limit are compared to the signal and an alarm signal must, therefore, appear on the output line of the system at the end of this period. The synchronization signal for the pulse generator must always be taken from the output of C 2 which corresponds to the channel under test.

The same method is used to test the monitoring of the lower limit, only in this case the pulse polarity must be reversed so that the composite signal is the difference of bias and pulse and as such smaller than the lower limit stored in the adaptor.

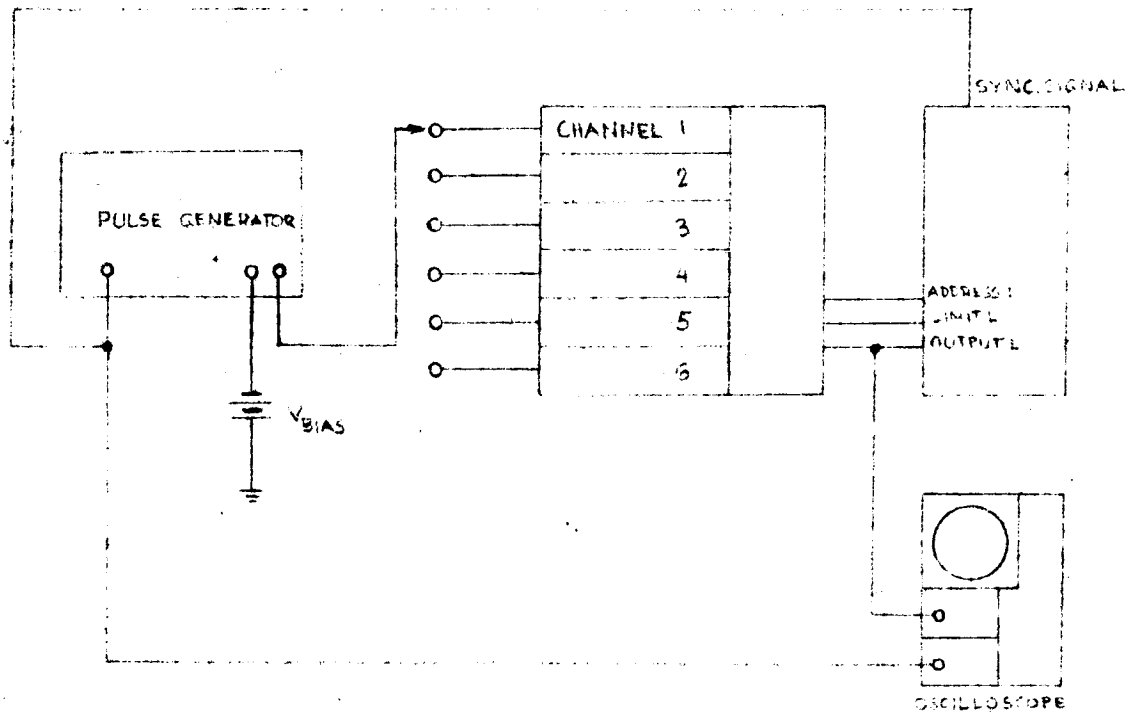

SYNC. SIGNAL
CHANNEL 1
2
3
4
5
6
PULSE GENERATOR
V_{BIAS}
OUTPUT
OSCILLOSCOPE

FIG.8.1

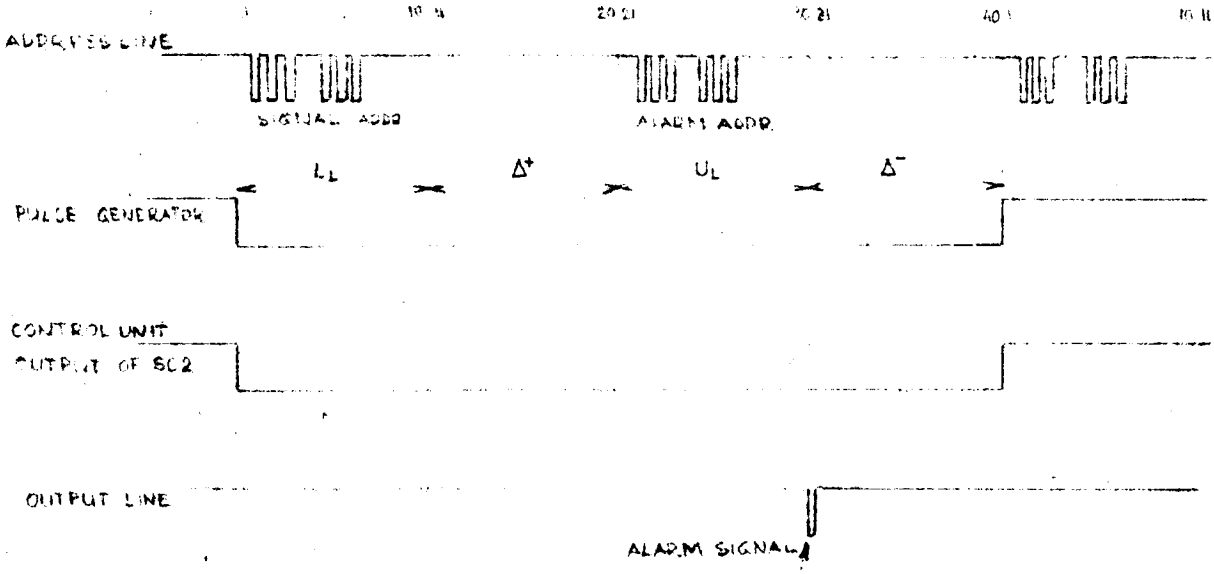

ADDRESS LINE
SIGNAL ADDR
ALARM ADDR.
L_L
Δ^+
U_L
Δ^-
PULSE GENERATOR
CONTROL UNIT
OUTPUT OF SC2
OUTPUT LINE
ALARM SIGNAL

FIG.8.2

Fig. 8.3 shows the setup for testing rate of change monitoring. Fig. 8.4 shows the time relationships of the pertinent wave shapes.

The signal applied to the adaptor under test consists of a DC voltage on which a ramp function is superimposed. The D C bias voltage is required to insure that neither of the amplitude limits are exceeded during the test. The slope of the ramp function is adjusted to a value just slightly longer than the the value which corresponds to the upper rate of change limit stored in the adaptor. The ramp voltage is started by the leading edge of the output signal from gate A 14 of the control unit. This signal is used to produce a command signal which causes the adaptor to shift a new value into its previous value register. The previous value register then retains this value for 40,000 clock pulses until it receives the next command signal. If the change of the input voltage with a slope which corresponds to a value slightly larger than the stored rate of change limit is started concurrently with the replacement of the contents of the previous value register, then an alarm is detected at the end of the 40,000 clock pulse interval and an alarm signal must appear immediately following the alarm address of the adaptor under test. By synchronizing the beginning of the ramp function with the replacement of the contents of the previous value register, ambiguity as to the exact time when an alarm has been detected is avoided.

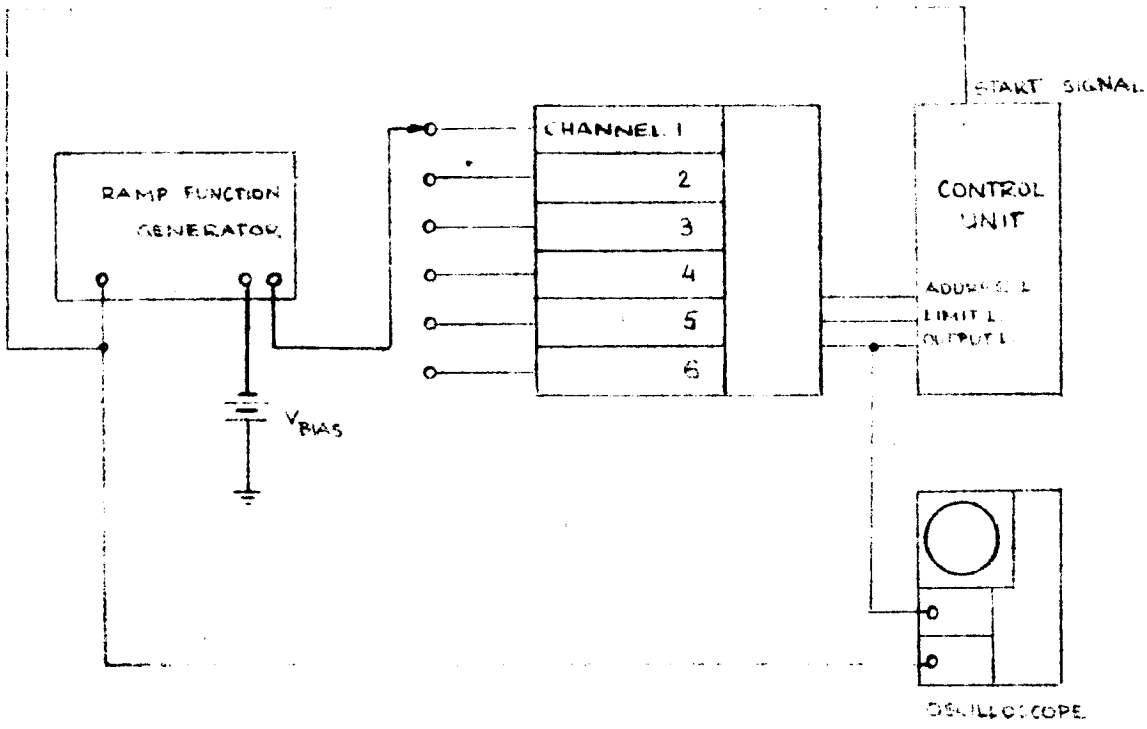

START SIGNAL
CHANNEL 1
2
3
4
5
6
RAMP FUNCTION GENERATOR
CONTROL UNIT
ADDRESS
LIMIT
OUTPUT
V_{BIAS}
OSCILLOSCOPE

FIG.8.3

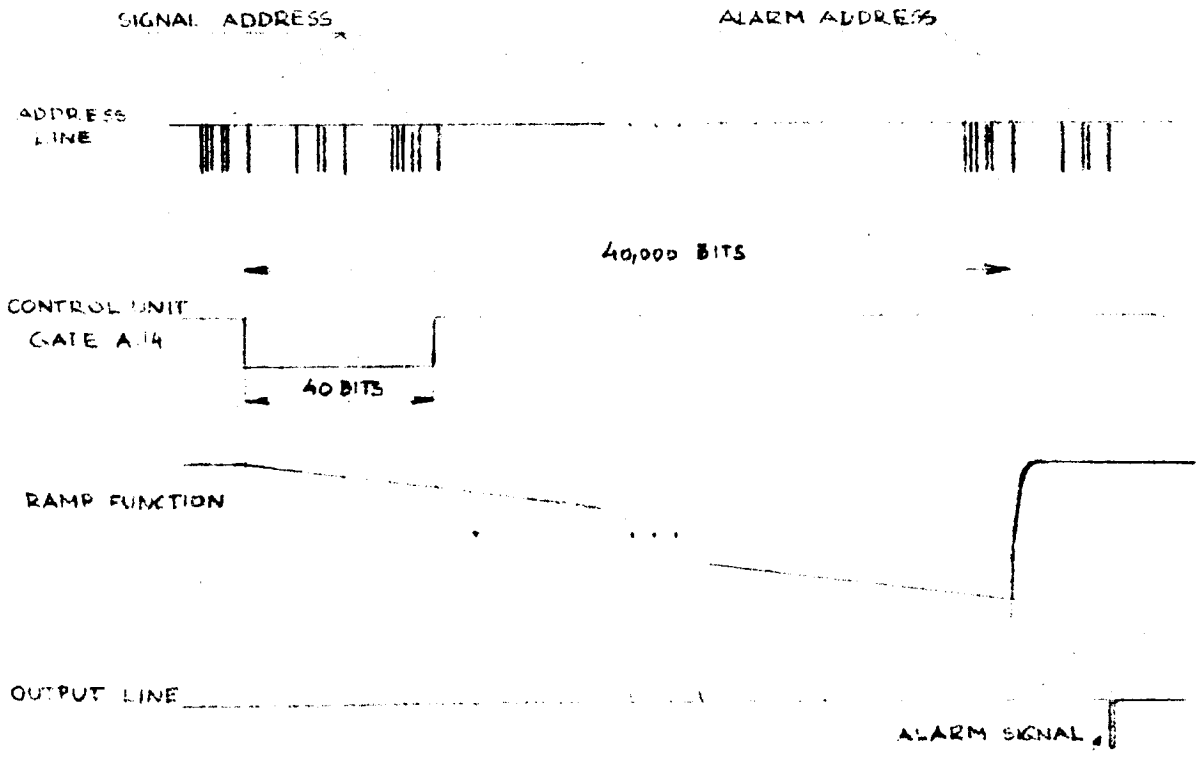

SIGNAL ADDRESS
ALARM ADDRESS
ADDRESS LINE
40,000 BITS
CONTROL UNIT GATE A 14
40 BITS
RAMP FUNCTION
OUTPUT LINE
ALARM SIGNAL

FIG.8.4

For, if we assume that the ramp voltage was started in the middle of the 40,000 clock pulse period, then it might take more than 60,000 clock pulses before an alarm signal is produced.

Lower rate of change limit monitoring is tested in the same manner, the difference being only the sign of the slope of the ramp function.

As experience increases after testing of the digital adaptor has been started, improved test methods will be found which eventually will find application in the checkout of installed systems using the digital adaptor for transducers.

9.0 COSTS OF MATERIALS

The costs of materials of one digital adaptor module, one manual limit loading box and the control unit for testing are shown below. The fourth cost breakdown shown below refers to a system with 6 channels which is proposed to be built to demonstrate the feasibility of the design concept of the digital adaptor for tansducers.

The cost of the system of six channels contains an amount for parts in excess of what is needed for the construction of the system (scrap). These parts will be needed for experiments and to serve as replacements for parts lost in manufacturing and testing. Only six A/D converters shown in the break down for these items are completely developed off-the-shelf models. It is not expected that any of them will be damaged or lost during manufacturing and testing.

DIGITAL ADAPTOR MODULE

Part	Number	Unit Price	Total Price
pL4G01	15	12.60	189.00
pL4G02	2	43.90	87.80
MEM1000	1	32.00	32.00
MEM1002	1	12.00	12.00
MEM1005	4	15.00	60.00
MEM3012SP	3	78.00	234.00
MEM3021	3	74.50	223.00
MEM4000	1	15.00	15.00
Patchboard connector	1	9.00	9.00
Patchboard plug	1	9.00	9.00
Limit box connector	1	3.00	3.00
Printed circuit board	1	3.00	3.00
Multilayer interconnections	20	2.50	50.00
ADC-10$_{ic}$ Converter	1	1000.00	1000.00
2N2222 transistor	3	3.98	11.92
2N2907 transistor	2	8.70	17.40
IN916 diode	4	.67	2.68
Resistors	13	.28	3.64
Miscellaneous			100.00
One Digital Adaptor Module			$2065.00

MANUAL LIMIT LOADING BOX

Part	Number	Unit Price	Total Price
MEM 1005	11	15.00	165.00
MEM 3021	2	74.50	149.00
pL4G01	1	12.60	12.60
2N2222	1	3.98	3.98
Resistors	3	.28	.84
Capacitor	1	1.34	1.34
Lever action switch	1	1.20	1.20
Toggle switch	1	.53	.53
Push button switch	12	.60	7.20
Case	1	1.32	1.32
Connector	1	3.00	3.00
Miscellaneous			30.00
One Manual Limit Loading Box			$380.00

CONTROL UNIT FOR TESTING

Part	Number	Unit Price	Total Price
pL4G01	5	57.50	287.50
pL4G01	16	12.60	201.60
pL4G02	2	43.90	87.80
MEM1005	3	15.00	45.00
MEM3012SP	1	78.00	78.00
MEM4000	1	15.00	15.00
IN916	9	.67	6.03
2N2907	5	8.70	43.50
2N2222	1	3.98	3.98
2N2905	1	3.00	3.00
Resistors	17	.28	4.76
Capacitor	1	1.34	1.34
Potentiometer	1	5.67	5.67
Incandescent bulbs	10	.31	3.10
Sockets	10	.31	3.10
Push button switch	1	.60	.60
Toggle switches	6	.53	3.18
Rotary switch	1	2.10	2.10
Case	1	1.65	1.65
Connectors	3	9.00	27.00
Miscellaneous			90.00
One Control Unit for Testing			$876.00

SYSTEM WITH 6 CHANNELS

Part	Number	Unit Price	Total Price
Digital adaptor	6	2065.00	12,390.00
Manual limit adj. box	1	380.00	380.00
Control unit	1	876.00	876.00
Scrap (10% except 6 A/D converters)			765.00
Material Cost			$14411.00

10.0 WORK PLANNED

After approval of the design of a digital adaptor for transducers resulting from Phase B effort, Phase C of the contract will be started. During this phase a system of six channels consisting of six adaptor modules, one manual limit loading box and one control unit for testing will be constructed.

Before the fabrication of all six adaptors is started, a breadboard model of the adaptor will be built to check the soundness of the design and of the interconnections.

The system will be thoroughly tested and the thus gained experience applied to the writing of the Acceptance Test Procedures.

Phase C will end with the delivery of a system of six adaptors and the acceptance test procedure.

11.0 COST SUMMARY AND PROJECTION OF FUTURE EXPENDITURES

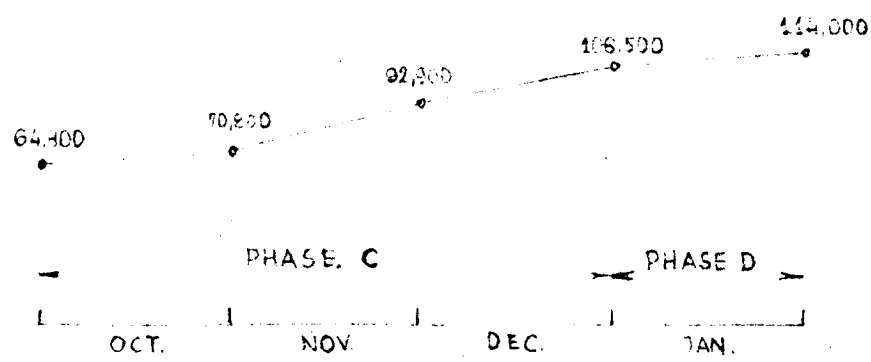
At the end of Phase B a total of $64,300 or 72% of the total costs funded for the contract have been expended. Of this amount $40,550 or 45% have been spent during Phase B alone.

Phase B, which comprises the main effort of the scope of work of the contract, required more time than originally anticipated. The reason for delay is to be found in the nature of the task which did not allow a division of work among many individuals. As it turned out, it was mainly a task for two engineers.

Difficulties developed when it became apparent that certain semiconductor devices which had been on the market when Phase B was started were no longer available. Design changes became unavoidable causing costly delays.

The projection of future expenditures reflects the effect of these delays and also the increased costs of materials which proved higher than originally anticipated.

Below, a graphical representation of the projection of future expenditures is given:



APPENDIX A

Theory of the Limit Comparator

Three numbers A, B, and C are given in binary form:

$$A = A_n 2^{n-1} + A_{n-1} 2^{n-2} \ldots A_2 2^1 + A_1 2^0 = \sum_{i=1}^{n} A_i 2^{i-1}$$

$$B = B_n 2^{n-1} + B_{n-1} 2^{n-2} \ldots B_2 2^1 + B_1 2^0 = \sum_{i=1}^{n} B_i 2^{i-1}$$

$$C = C_n 2^{n-1} + C_{n-1} 2^{n-2} \ldots C_2 2^1 + C_1 2^0 = \sum_{i=1}^{n} C_i 2^{i-1}$$

We want to compare A to the sum B + C by examining, step by step, the sets of bits (A_i B_i C_i) of the same position beginning with the most significant bits. We want to know whether $A > B + C$ or $A \leq B + C$ with the least number of steps.

I.) $A = B + C$ if $A_i = B_i + C_i$ for $i = 1, 2, \ldots n$

or $A_i = B_i = 1$, $C_i = 0$

$A_i = C_i = 1$, $B_i = 0$ (1)

$A_i = B_i = C_i = 0$

Rewriting A, B, and C:

$$A = \sum_{i=d+1}^{n} A_i 2^{i-1} + \sum_{i=1}^{d} A_i 2^{i-1}$$

$$B = \sum_{i=d+1}^{n} B_i 2^{i-1} + \sum_{i=1}^{d} B_i 2^{i-1}$$

$$C = \sum_{i=d+1}^{n} C_i 2^{i-1} + \sum_{i=1}^{d} C_i 2^{i-1}$$

If $A_i = B_i + C_i$, $i = d + 1, \ldots n$ then the first n - d bits will not decide whether $A > B + C$ or $A \leq B + C$. If we meet with the condition $A_i = B_i + C_i$ for $i = d + 1 \ldots n$ we can disregard these portions of the numbers in the following considerations. It suffices to consider only numbers for which $A_d \neq B_d + C_d$ for the most significant bit.

2.) $A < B + C$

If $A_d < B_d + C_d$ or $A_d = B_d = 0,\ C_d = 1$

$A_d = C_d = 0,\ B_d = 1$

$A_d = 0,\ B_d = C_d = 1$ (2)

$A_d = B_d = C_d = 1$

For: $$2^{d-1} > \sum_{i=1}^{d-1} A_i\, 2^{i-1}$$

$$(A_d + 1)\, 2^{d-1} > \sum_{i=1}^{d} A_i\, 2^{i-1}$$

from (2): $$(B_d + C_d)\ 2^{d-1} \geq (A_d + 1)\, 2^{d-1} > \sum_{i=1}^{d} A_i\, 2^{i-1}$$

$$\sum_{i=1}^{d}(B_d + C_d)\, 2^{i-1} \geq (B_d + C_d)\, 2^{d-1} > \sum_{i=1}^{d} A_i\, 2^{i-1}$$

$$\sum_{i=1}^{d}(B_d + C_d)\, 2^{i-1} > \sum_{i=1}^{d} A_i\, 2^{i-1} \quad \text{q. e. d.}$$

3. $A > B + C$

If $A_c > B_d + C_d$ or $A_d = 1,\ B_d = C_d = 0$ (3)

$B_j + C_j = A_j + 1$, or $A_j = B_j = 0,\ C_j = 1$

$j = g+1, \ldots d-1$ $\quad A_j = C_j = 0,\ B_j = 1$ (4)

$A_j = B_j = C_j = 1$

$A_g \geq B_g + C_g$ or $A_g = B_g = C_g = 0$

$A_g = B_g = 1,\ C_g = 0$

$A_g = C_g = 1,\ B_g = 0$ (5)

$A_g = 1,\ B_g = C_g = 0$

For from (4) : $$\sum_{j=g+1}^{d-1}(B_d + C_d)2^{j-1} = \sum_{j=g+1}^{d-1} A_j 2^{j-1} + \sum_{j=g+1}^{d-1} 2^{j-1} \quad (6)$$

from (3) $A_d\, 2^{d-1} = 2^{d-1} > \sum_{j=g+1}^{d-1} 2^{j-1}$

from (3): $\sum_{j=g+1}^{d-1} (B_j + C_j)\, 2^{j-1} = \sum_{j=g+1}^{d} (B_j + C_j)\, 2^{j-1}$

$$\sum_{j=g+1}^{d} (B_j + C_j)\, 2^{j-1} = \sum_{j=g+1}^{d-1} A_j\, 2^{j-1} + \sum_{j=g+1}^{d-1} 2^{j-1}$$

from (6): $\sum_{j=g+1}^{d} (B_j + C_j)\, 2^{j-1} - \sum_{j=g+1}^{d-1} A_j\, 2^{j-1} = \sum_{j=g+1}^{d-1} 2^{j-1}$

from (3): $A_d\, 2^{d-1} = 2^{d-1}$

$$2^{d-1} - \sum_{j=g+1}^{d-1} 2^{j-1} = 2^g$$

$$\sum_{j=g+1}^{d} A_j\, 2^{j-1} - \sum_{j=g+1}^{d} (B_j + C_j)\, 2^{j-1} = 2^{d-1} - \sum_{j=g+1}^{d-1} 2^{j-1} = 2^g \qquad (7)$$

from (5): $A_g\, 2^{g-1} - (B_g + C_g)\, 2^{g-1} \geq 0 \qquad (8)$

$$\sum_{k=1}^{g-1} (B_k + C_k)\, 2^{k-1} \leq 2 \sum_{k=1}^{g-1} 2^{k-1} = \sum_{k=2}^{g} 2^{k-1}$$

$$\sum_{k=1}^{g-1} A_k\, 2^{k-1} - \sum_{K-1}^{g-1} (B_k + C_k)\, 2^{k-1} \geq -\sum_{K=2}^{g} 2^{k-1} \qquad (9)$$

Adding (7) (8) (9) $\sum_{h=1}^{d} A_h\, 2^{h-1} - \sum_{h=1}^{d} (B_h + C_h)\, 2^{h-1} \geq 2^g - \sum_{K=2}^{g} 2^{k-1}$

It is now possible to derive logic equations for a comparator which accepts 3 binary numbers in serial form with the most significant bit first and which signals the condition A > B + C called "alarm".

The bits in the same position of the three numbers occur in any one of 8 combinations as shown in Table I.

Combination	A_i	B_i	C_i
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	0
5	1	0	1
6	0	1	1
7	1	1	1
8	0	0	1

TABLE I.

Combinations 3, 4, and 5,when occuring first, correspond to equation 1.): written in Boolean algebra:

$$S = A_i B_i \bar{C}_i + \bar{A}_i \bar{B}_i \bar{C}_i + A_i \bar{B}_i C_i$$

The comparator remains in its initial state when any of the combinations 2, 6, 7, and 8 occur after only combinations 3, 4, and 5 have occured then A < B + C (equations (2)). In Boolean algebra:

$$N = \bar{A}_i B_i \bar{C}_i + \bar{A}_i B_i C_i + A_i B_i C_i + \bar{A}_i \bar{B}_i C_i \qquad (14)$$

Regardless of what combinations follow, A cannot exceed B + C. The comparator, therefore, must be inhibited from going into the alarm state during the remaining part of the comparison cycle.

If combination 1 occurs after only combinations 3, 4, and 5 have occured then it is possible but <u>not certain</u> yet that A > B+C. (equation 3)

Written as a logic equation

$$A_1 = A_i \bar{B}_i \bar{C}_i \qquad (15)$$

As long as only combinations 2, 7, and 8 (equation 4) occur after combination 1, no decision can be made. But if any of the combinations 1, 3, 4, and 5 (equation 5) occur after 2, 7, and 8, then A > B + C and the comparator must produce an alarm signal.

The logic condition is:

$$A_2 = A_j \bar{B}_j \bar{C}_j + A_j B_j \bar{C}_j + A_j \bar{B}_j C_j + \bar{A}_j \bar{B}_j \bar{C}_j \qquad (16)$$

$$\bar{A}_2 = \overline{A_j \bar{B}_j \bar{C}_j + A_j B_j \bar{C}_j + A_j \bar{B}_j C_j + \bar{A}_j \bar{B}_j \bar{C}_j} =$$

$$= (\bar{A}_j+B_j+C_j)(\bar{A}_j+\bar{B}_j+C_j)(\bar{A}_j+B_j+\bar{C}_j)(A_j+B_j+C_j) =$$

$$= \bar{A}_j B_j \bar{C}_j + \bar{A}_j B_j C_j + A_j B_j C_j + \bar{A}_j \bar{B}_j C_j$$

Therefore $\bar{A}_2 = \bar{N}$ (17)

If combination 6 occurs instead of any of combinations 1, 3, 4, and 5 then the comparator must be reset to its initial state.

Combination 6 is written as:

$$R = \bar{A}_j \, B_j \, C_j \qquad (18)$$

The comparator must detect $C > P + \Delta+$ during rate of change monitoring. C is the current value of the measurand obtained from the A/D converter, P is the previous value of the measurand stored in the previous value register and Δ^+ is the maximum allowable change of the measurand in the time interval

Setting $C = A$

$P = B$

$\Delta^+ = C$

We have all the needed functions for comparison in equations 14 through 18. Certainly no alarm (equation 14):

$$N = C \, P\Delta^+ + \bar{C} \, P\Delta^+ + \bar{C} \, \bar{P}\Delta^+ + \bar{C} \, P \, \bar{\Delta}^+ \qquad (19)$$

This function can be implemented by a 3 input majority gate and applying $\bar{C}$ instead of C.

The inverted output of this majority gate equals function A_2 (equations 16 and 17)

$A_1 = C \, \bar{P} \, \bar{\Delta}^+$ (equation 15) can be implemented by a 3 input NOR gate and applying again $\bar{C}$ instead of C.

$$A_1 = \overline{(\bar{C} + P + \Delta^+)} = C \, \bar{P} \, \bar{\Delta}^+$$

$R = \bar{C} \, P\Delta^+$ (equation 17) can be implemented by a 3 input A N D gate and applying $\bar{C}$ instead of C.

Fig. I shows the block diagram of a comparator meeting the

above conditions.

Flip - flops FF_1 and FF_2 and register R_1 initally are in the "0" state, and the outputs of NOR_2 and A_2 are "0". When condition N occurs the output of N and A_2 become "1", FF_2 is set thereby applying a "1" to NOR_2.

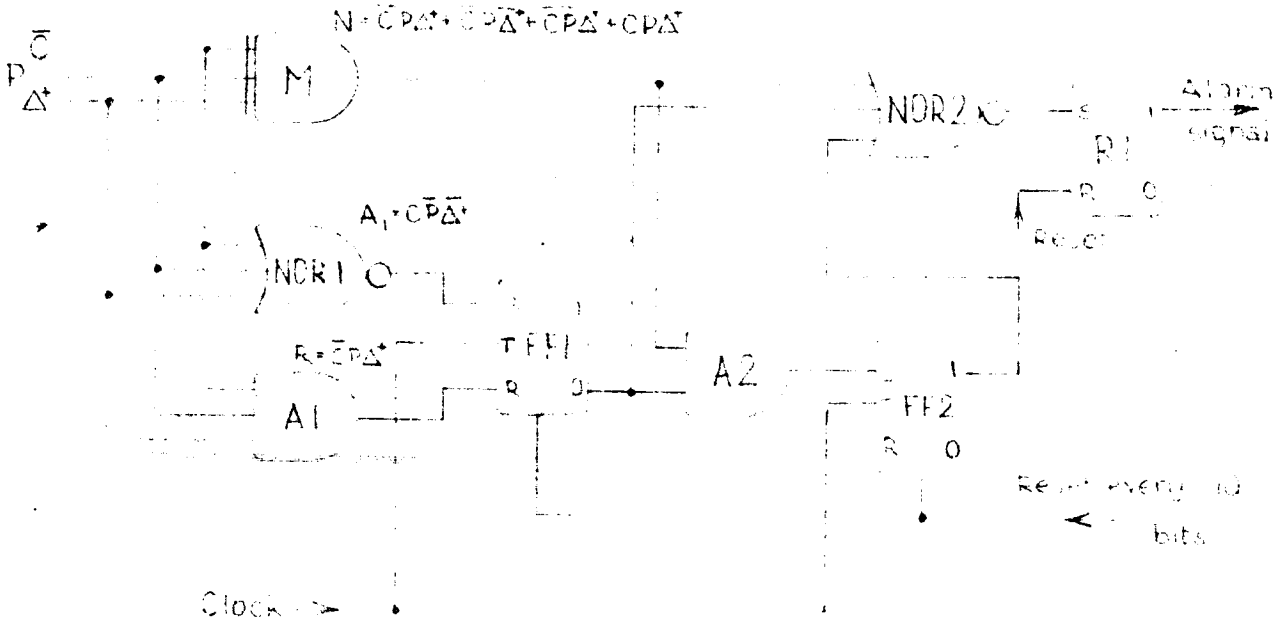


Figure 1.

As long as FF_2 is not reset no signal can reach R_1 because of the "1" applied to one of the inputs of NOR_2. No combination of C, P, and Δ^+ can now influence the state of R_1. After the least significant bits of C, P, and Δ^+ have been applied to the comparator, it is reset and ready for the next comparison cycle.

When an A_1 condition occurs then the output of M is "0" and the output of NOR_1 is "1". The next clock pulse sets FF_1 to "1". Two inputs of NOR_2 are now at "0". If M is also "0" (if condition A_2 exists) then the output of NOR_2 is "1" and sets R_1 to "1" which indicates an alarm condition. Once R_1 is set it can only be reset by a command derived from other circuits of the adapter.

Any condition other than A_2 and R following A_1 will not influence the state of the comparator and when eventually followed by A_2 will produce an alarm. However, if R occurs instead of A_2 then AND gate A_1 will be "1" and the next clock pulse will clear FF1. The comparator is then again in its initial state and will produce an alarm signal depending on the remaining bits of C, P, and Δ^+.

Every 10 bits - after one comparison - the comparator is reset. If condition A_1 occurs during the last bit no alarm signal is produced inspite of the fact that the limit is exceeded by 1.

The comparator can only produce an alarm signal if both conditions A_1 and A_2 have occured. In the case of the last bits corresponding to condition A_1 this is not possible. Therefore, an alarm is only produced if the limit has been exceeded by at least 2 (equation 10).

It remains to be shown that a negative rate of change, upper limit UL and lower limit LL can also be monitored by the same circuit.

Negative rate of change is exceeded if

$$C < P - \Delta^- \quad \text{or}$$

$$C + \Delta^- < P$$

Before we had $P + \Delta^+ < C$. Comparing these 2 unequalities we recognize that P and C changed places. Therefore, all that is required for negative rate of change monitoring is applying $\bar{P}$ instead of P and C instead of $\bar{C}$ to the comparator. A circuit which alternately complements P and C before they are applied to the comparator will suffice.

Upper limit is exceeded if

$$C > UL$$

UL is stored in the same register as Δ^+ and Δ^- and appears on the same line. Therefore, $C > UL$ is detected by keeping the P input of the comparator at "C" during this comparison cycle.

Lower limit is exceeded if

$$C < LL$$

$$\text{Or} \quad \bar{C} > \overline{LL}$$

This function is obtained by applying C instead of $\bar{C}$ to the comparator, keeping its P input at "0" and storing the complement of the lower limit, $\overline{LL}$ in the limit register.

Because of equation 10 and resetting of the comparator every ten bits an alarm is only produced if the limits are exceeded by 2 units. This can be corrected by storing $\Delta^+ - 1$, $\Delta^- - 1$, UL - 1, and $\overline{LL}$ - 1 in the adapter.

APPENDIX B

TIME TABLE 1 SILENT MODE

During the preceeding 10 bits and address word was shifted into SR 4 and SR 5. This address does not activate the output of the adaptor. During the following 40 bits RG 1, RG 3, RG 4, and FF 3 remain reset. The outputs of A 6, A 7, A 12, A 13, A 14, A 16, A 17, OR 12, and the inverted output of OR 4 remain at "0" and the outputs of OR 1, OR 5, and OR 10 remain at "1".

BIT	
1	Signal address received (module not addressed). Outputs 1 and 9 of SR 4 and outputs of A 11 and OR 9 are "1". FF 5 and RG 2 are set, FF 1 and RG 5 are reset. Output of A 10 and the inverted output of A 5 are "0". The inverted outputs of OR 7 and OR 8 are not both "1" and, therefore, A 9 is "0". A "1" is placed into SR 3. A/D converter is reset and started with the most significant bit first.
2	Output 0 of SR 4 goes to "1", setting FF 4 which in turn resets both SR 4 and SR 5 immediately. Output of A 11 goes to 0.
3	FF 4 is reset.
1...10	10 "0's" are shifted into SR 4 and SR 5. Current value is compared to previous value plus Δ^+. Current value from A/D converter is inverted by OE 1 (second input is "1") and

BIT	fed to the comparator gates M, A 2 and OR 3. Previous value from SR 2 and Δ^+ from the inverted output of A 15 are also fed to these gates. Previous value is inverted by A 1 (second input is "1" from OR 1) and recirculated. The complement of Δ^+ is shifted out of SR 1, inverted by A 15 and recirculated after a second inversion by A 4.
11	Outputs of SR 3 and OR 9 are "1" resetting FF 1, RG 2, and RG 5. Inverted output of A 5 is "1". A/D converter is reset and started with the most significant bit first.
11...20	Alarm address is shifted into SR 4 and SR 5. Current value is compared to upper limit. Current value from A/D converter is inverted by OE 1 (second input is "1") and fed to the comparator gates M, A 2 and OR 3. Upper limit from the inverted output of A 15 is also fed to these gates. The output of SR 2 is "0" during this period. Because the inverted output of A 5 is "1", OR 2 is also "1" causing the inverted output of A 1 to stay at "0" thereby placing 10 "0's" into SR 2. Upper limit is recirculated the same way as Δ^+.

BIT	
21	Alarm address received (module not addressed). Output 1 of SR 4 and outputs of A 10 and OR 9 are "1". FF 1, FF 5, and RG 5 are reset. RG 2 is set. Inverted output of A 5 is "0". The inverted outputs of OR 7 and OR 8 are not both "1" and, therefore, A 9 is "0". A "1" is placed into SR 3. The A/D converter is reset and started with the most significant bit first.
22	Output 0 of SR 4 goes to "1", setting FF 4 which in turn resets both SR 4 and SR 5 immediately. Output of A 10 goes to "0".
23	FF 4 is reset.
21...30	10 "0's" are shifted into SR 4 and SR 5. Current value is compared to previous value minus Δ^-. Current value from A/D converter passes OE 1 unchanged (second input of OE 1 from FF 5 is "0") and is fed to comparator gates M, A 2 and OR 3. The complement of the previous value from SR 2 and Δ^- from the inverted output of A 15 are also fed to these gates. Complement of previous value is inverted by A 1 (second input is "1" from OR 1)

BIT	
	and recirculated. The complement of Δ^- is shifted out of SR 1, inverted by A 15 and recirculated after a second inversion by A 4.
31	Outputs of SR 3 and OR 9 are "1" resetting FF 1, RG 2, and RG 5. Inverted output of A 5 is "1". A/D converter is reset and started with the most significant bit first.
31...40	Signal address is shifted into SR 4 and SR 5. Current value is compared to lower limit. Current value from A/D converter passes OE 1 unchanged (second input of OE 1 from FF 5 is "0") and is fed to comparator gates M, A 2, and OR 3. The complement of the lower limit from the inverted output of A 15 is also fed to these gates. The output of SR 2 is "0" during this period. Because the inverted output of A 5 is "1" OR 2 is also "1" causing the inverted output of A 1 to stay at "0" thereby placing 10 "0's" into SR 2. The complement of the lower limit is recirculated the same way as Δ^-.
40	One comparison cycle is completed.

After every 100,000th clock pulse (or once a second) the contents of the previous value register SR 2 are replaced by the current value put out by the A/D converter upon receiving a command signal.

BIT

100,001;200,001:... 100,000 j + 1	Time base synchronization signal received (module addressed or not addressed). Outputs 1, 9, and 10 of SR 4 are "1". Output of A 13 is "1". RG 4 is set. Inverted output of A 5 is "1".
100,001...100,010 200,001...100,010 100,000 j + 1... 100,000 j + 10	Current value from A/D converter is inverted and shifted into SR 2. The inverted output of A 5 stays "1" during this period, blocking recirculation of previous value stored in SR 2 through OR 2 (inverted output of A 5 is "1") OR 1 allows current value to pass (its second input is "0"). A 1 inverts the current value before it is shifted into SR 2. All other events are the same as during the silent - or if the module has been addressed - active mode.
100,011;200,011;... 100,000 j + 11:...	Output of Sr 3 is "1" resetting RG 4. Cutput of OR 1 is "1" preventing the output of the A/D converter from entering SR 2. All other events are the same as during silent or active mode.

TIME TABLE 2 ACTIVE MODE

During the preceding 10 bits the module's own signal address was shifted into SR 4 and SR 5. During the following 10 bits RG 1 RG 4, and FF 3 remain reset, RG 2 and FF 5 remain set. The outputs of A 7, A 10, A 12, A 13, and A 14, and the inverted outputs of A 5 and OR 4 remain at "0". The outputs of OR 1, OR 5, and OR 10 remain at "1".

BIT	
40k + 1	Signal address received (module addressed) outputs 1 and 9 of SR 4 and outputs of A 11 and OR 9 are "1". FF 5 and RG 2 are set, FF 1 and RG 5 are reset. Output of A 10 and the inverted output of A 5 are "0". A "1" is placed into SR 3. The inverted outputs of both, OR 7 and OR 8, the outputs of A9, A 16 and A 17 are "1". RG 1 is reset (if it was set before), RG 3 is set. A 6 is enabled. A/D converter is reset and started with the most significant bit first.
40k + 2	Output 0 of SR 4 goes to "1", setting FF 4 which in turn resets both SR 4 and SR 5 immediately. Outputs of A 11, A 16 and A 17 go to "0".
40k + 3	FF 4 is reset.

BIT	
40k + 1...40k + 10	Current value is shifted out on the signal line through A 6 and OR 12. All other events are the same as during silent mode.
40k + 11	Output of SR 3 is "1" RG 3 is reset, A 6 is disabled. Active mode is completed. All other events are the same as during silent mode.

TIME TABLE 3 ALARM MODE

One of the limits was exceeded (an alarm had occured) and a "1" was placed into RG 1. This event may occur at any time during a comparison cycle except during bits 1, 11, 21, and 31 when FF 1 and RG 5 are being reset. If the number of channels of the system is m, it might take up to 40 m bits before the module receives its own alarm address. It is assumed that the module does not receive its own signal address until after having received its own alarm address. Consequently, RG 3 and FF 3 stay reset, A 16 and A 17 remain at "0" and A 6 is disabled.

BIT	
40(n-1) + 21...	A limit was exceeded and RG 1 is set to "1".
40(n+m) + 20	
40(n+m) + 21	Alarm address received (module addressed). Output 1 of SR 4 is "1", outputs 9 and 10 are "0". Outputs of A 10 and OR 9 are "1". FF 1, FF 5, and RG 5 are reset. RG 2 is set. The inverted output of A 5 is "0". The inverted outputs of OR 7 and OR 8 and the output of A 9 are "1". The outputs of A 7 and OR 12 are "1", an alarm signal appears on the signal line. A "1" is placed into SR 3. The A/D converter is reset and started with the most significant bit first.

BIT	
40(n+m) + 22	Output 0 of SR 4 goes to "1" setting FF 4 which in turn resets both SR 4 and SR 5 immediately. Outputs of A 7, A 10 and OR 12 go to "0".
40(n+m) + 23	FF 4 is reset. An alarm signal will be produced after every 40mth bit until the module has received its own signal address which then resets RG 1.

TIME TABLE 4 LIMIT LOADING

Limit loading takes place during the 40 bits following the module's own alarm address (bit 10 must be a "1"). While the limits are replaced step by step, the module continues to function undisturbed. It can be in any of the three other modes.

BIT	
40p + 21	Alarm address received (module addressed). Outputs 1 and 10 of SR 4 and outputs of A 10, A 12, and OR 9 are "1". The inverted outputs of OR 7 and OR 8 and the output of A 9 are "1". The output of A 14 is "1" setting FF 3. OR 6 is "1".
40p + 22	Output 0 of SR 4 goes to "1", setting FF 4 which in turn resets both SR 4 and SR 5 immediately. Outputs of A 10, A 12 and A 14 go to "0".
40p + 23	FF 4 is reset.
40p + 21...	Recirculation of the contents of SR 1 is interrupted and the new limits are shifted through OR 5 (second input from FF 3 is "0"), inverted by A 4 and entered into SR 1. The sequence of the limits being entered is Δ^- complement of lower limit $\overline{LL}$, Δ^+, upper limit UL.

BIT	
40 (p+1) + 21	Alarm address received (module addressed or not addressed). Output 1 of SR 4 and outputs of A 10 and OR 9 are "1". FF 5 is reset therby resetting FF 3. Output of OR 5 is "1" blocking further signals from the limit line. Contents of SR 1 are recirculated through OR 6. Limit loading is completed. All other events are the same as during silent - or if the module has been addressed - active mode.

FIG.B1 SILENT MODE

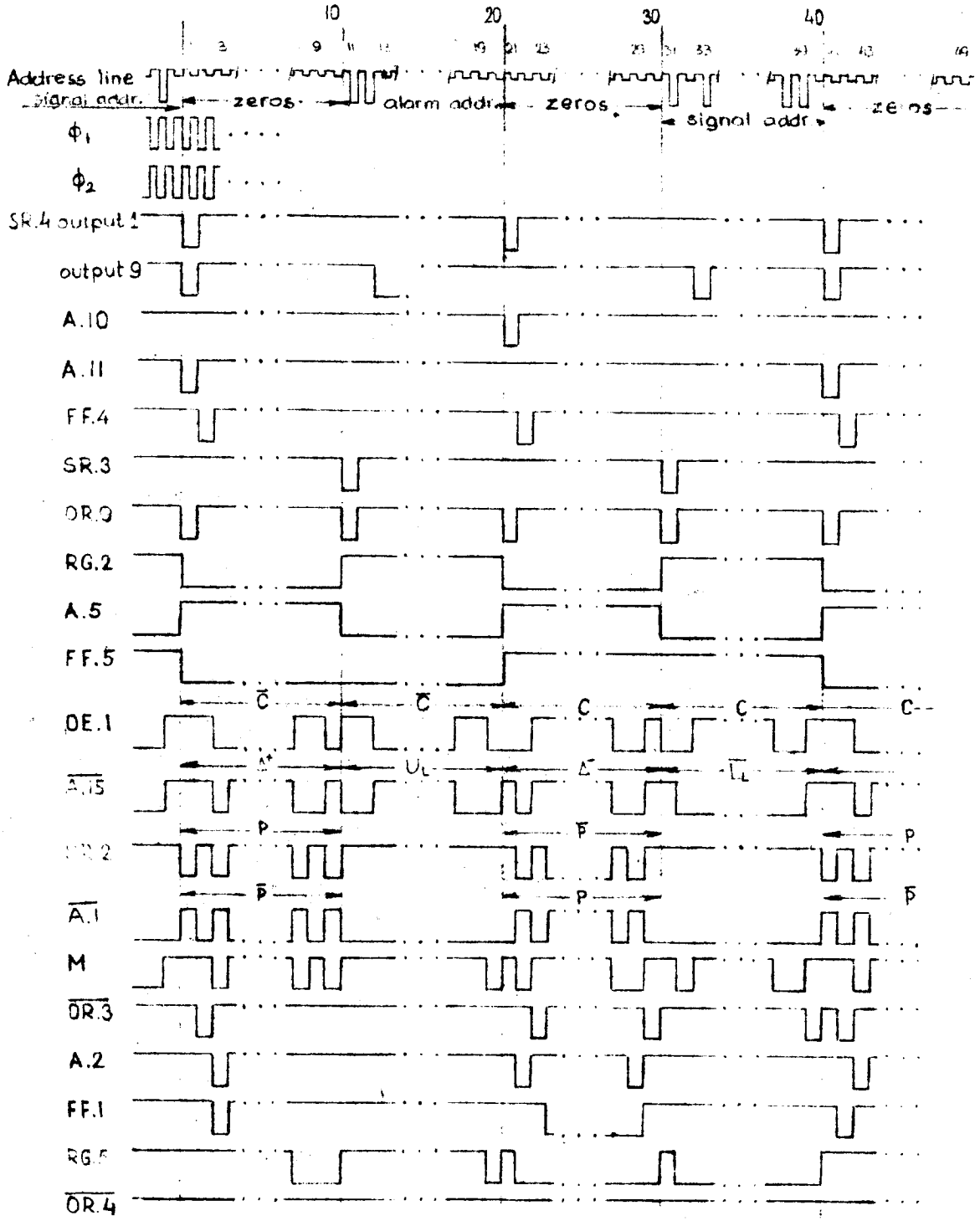


FIG.B2 ACTIVE MODE

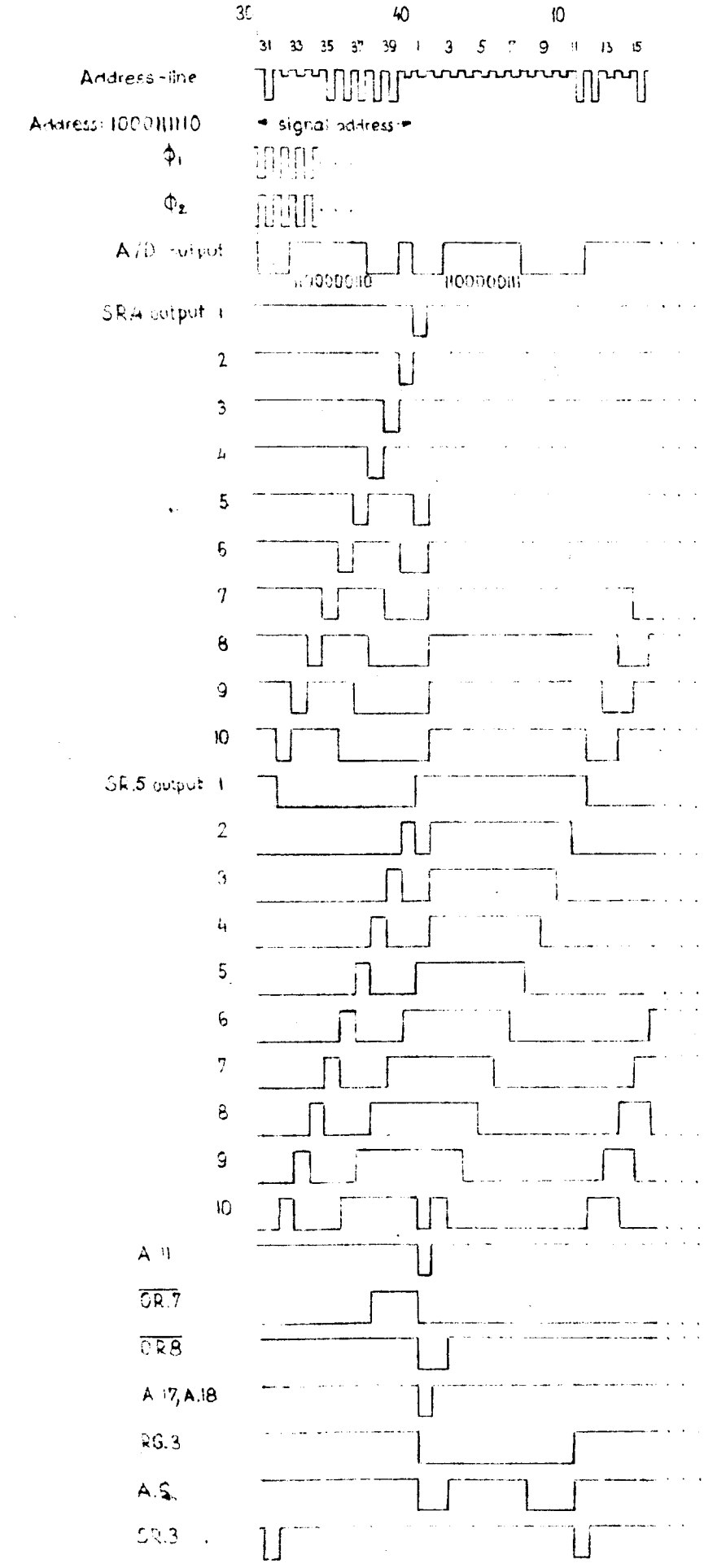


FIG.B3 ALARM MODE

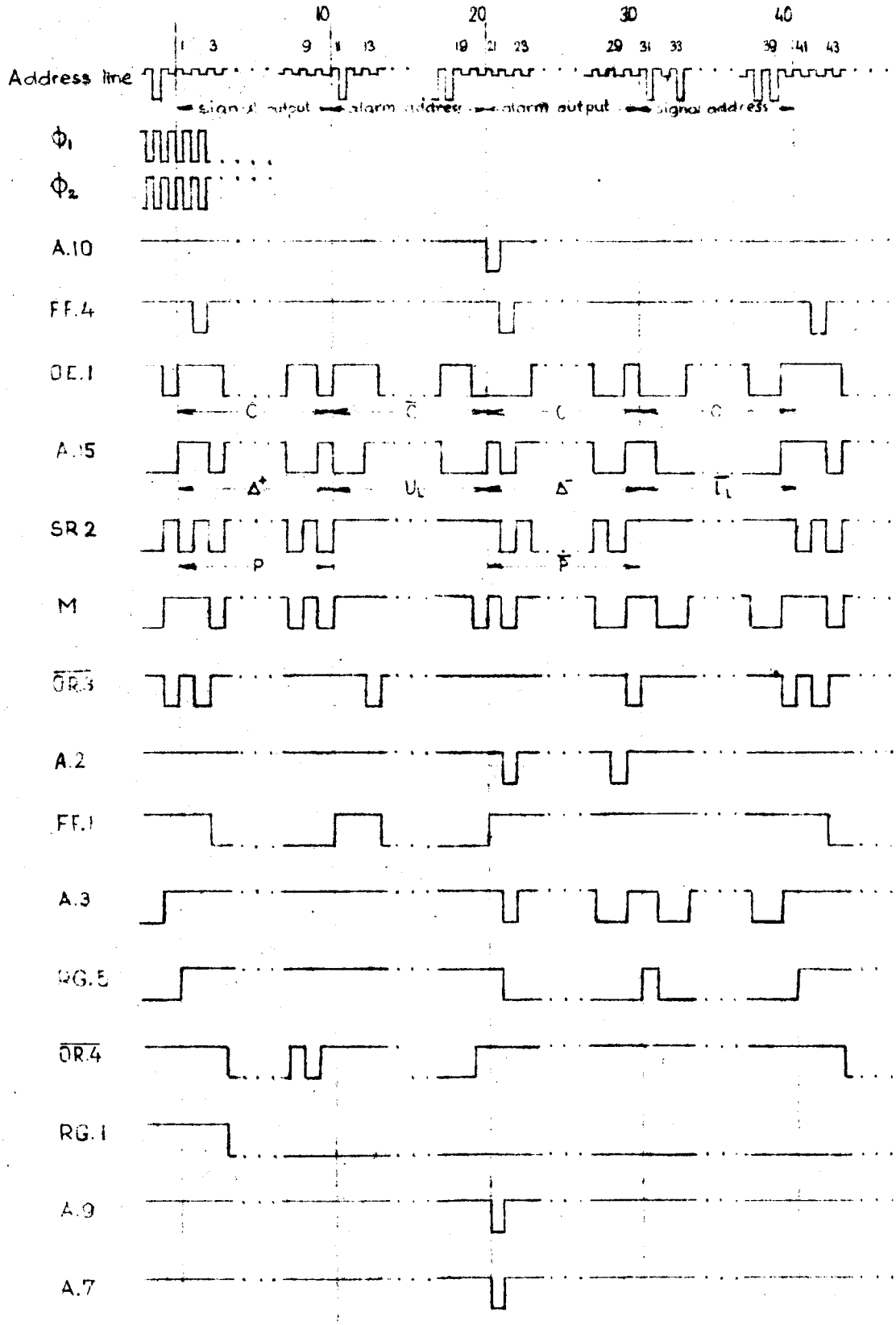
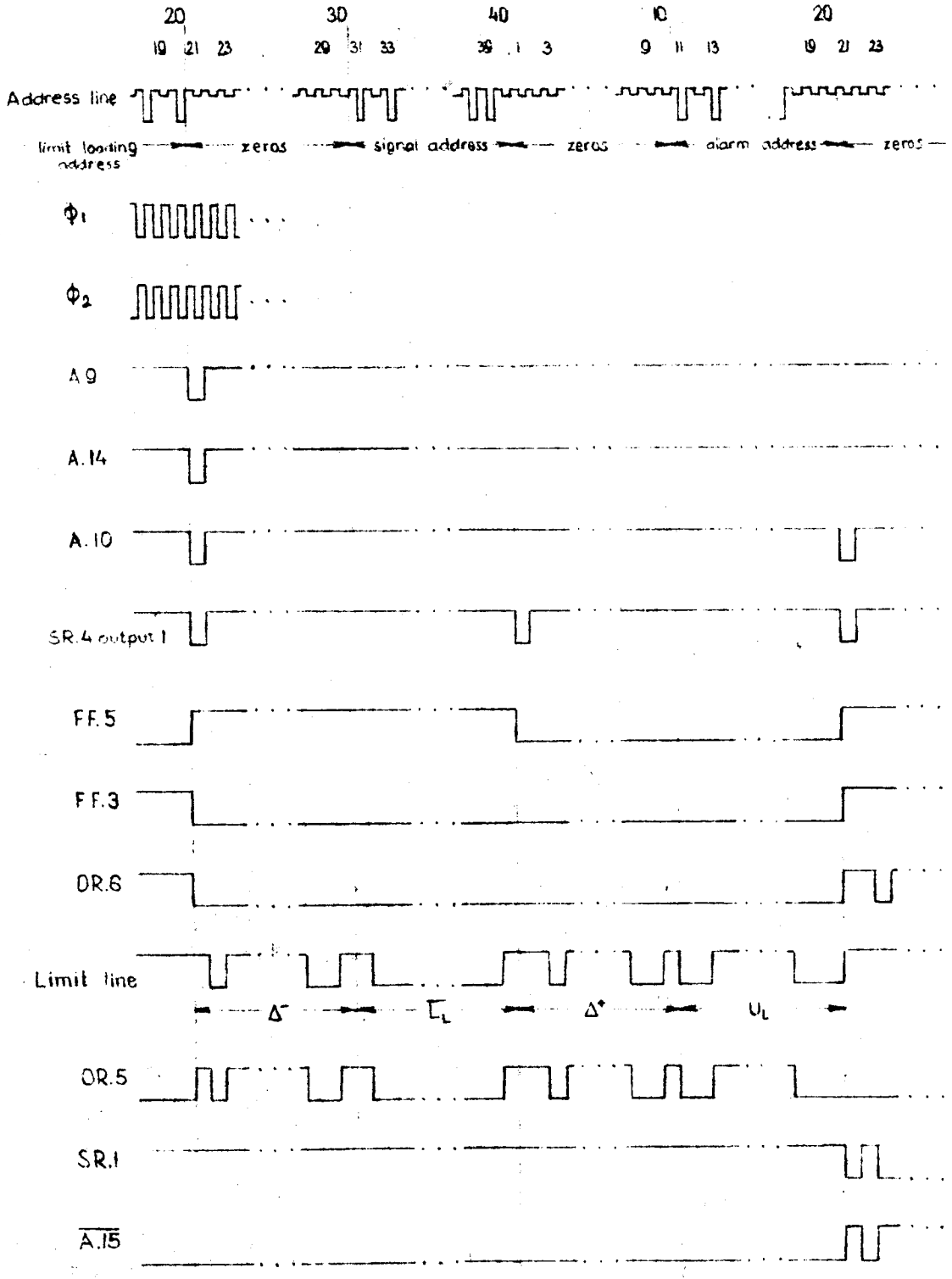


FIG B.4 LIMIT LOADING MODE



Appendix E

DIGITAL ADAPTER FOR TRANSDUCERS

PARTS LIST

According to Location on Schematic Diagram

Module Number	Function on Logic Diagram	Part Number	Manufacturer
1	A1, A5, OR1, OR2	pL4G01	Philco
2	OE1, M	MEM1000	General Instr.
3	A4, A15, OR5, OR6, OR10, OR11	pL4G01	Philco
4	FF3	MEM1005	General Instr.
5	SR2	MEM3021	General Instr.
6	A2	pL4G02	Philco
7	SR1/1	MEM3021	General Instr.
8	FF5	MEM1005	General Instr.
9	OR3, OR4	MEM1002	General Instr.
10	I2, I3	pL4G01	Philco
11	SR1/2	MEM3021	General Instr.
12	A14	pL4G01	Philco
13	A16, RG1	pL4G01	Philco
14	FF1	MEM1005	General Instr.
15	RG2	pL4G01	Philco
16	A10, A11, A12, A13	pL4G02	Philco
17	A7	pL4G01	Philco
18	A3, A8, RG5	pL4G01	Philco
19	RG4	pL4G01	Philco
20	OR7	pL4G01	Philco
21	OR8	pL4G01	Philco
22	A6	pL4G01	Philco

Module Number	Function on Logic Diagram	Part Number	Manufacturer
23	A17,RG3	pL4G01	Philco
24	OR9	pL4G01	Philco
25	SR4	MEM3012SP	General Instr.
26	SR5	MEM3012SP	General Instr.
27	AR1,AR2,AR3	MEM4000	General Instr.
28	SR3	MEM3012SP	General Instr.
29	FF4	MEM1005	General Instr.
30	I1	pL4G01	Philco
31	OR12	2xIN916	Texas Instr.
32	A/D Converter	ADC-10_{IC}	Pastoriza,Inc.

Appendix E

DIGITAL ADAPTOR FOR TRANSDUCERS

PARTS LIST

According to Function

Designation	Location On Schematic Diagram	Part Number	Manufacturer
A/D converter	31	ADC-10$_{ic}$	Pastoriza, Inc.
A1	1	pL4G01	Philco
A2	6	pL4G02	Philco
A3	18	pL4G01	Philco
A4	3	pL4G01	Philco
A5	1	pL4G01	Philco
A6	22	pL4G01	Philco
A7	17	pL4G01	Philco
A8	18	pL4G01	Philco
A9		connection	
A10	16	pL4G02	Philco
A11	16	pL4G02	Philco
A12	16	pL4G02	Philco
A13	16	pL4G02	Philco
A14	12	pL4G01	Philco
A15	3	pL4G01	Philco
A16	13	pL4G01	Philco
A17	23	pL4G01	Philco
M	2	MEM1000	General Instr.
OE1	2	MEM1000	General Instr.
OR1	1	pL4G01	Philco

Designation	Location On Schematic Diagram	Part Number	Manufacturer
OR2	1	pL4G01	Philco
OR3	9	MEM1002	General Instr.
OR4	9	MEM1002	General Instr.
OR5	3	pL4G01	Philco
OR6	3	pL4G01	Philco
OR7	20	pL4G01	Philco
OR8	21	pL4G01	Philco
OR9	24	pL4G01	Philco
OR10	3	pL4G01	Philco
OR11	3	pL4G01	Philco
OR12	31	2xIN916	Texas Instr.
SR1 (SR1-1&SR1-2)	7 & 11	2xMEM3021	General Instr.
SR2	5	MEM3021	General Instr.
SR3	28	MEM3012SP	General Instr.
SR4	25	MEM3012SP	General Instr.
SR5	26	MEM3012SP	General Instr.
FF1	14	MEM1005	General Instr.
FF3	4	MEM1005	General Instr.
FF4	29	MEM1005	General Instr.
FF5	8	MEM1005	General Instr.
RG1	13	pL4G01	Philco
RG2	15	pL4G01	Philco
RG3	23	pL4G01	Philco
RG4	19	pL4G01	Philco
RG5	18	pL4G01	Philco

Designation	Location On Schematic Diagram	Part Number	Manufacturer
I1	30	pL4G01	Philco
I2	10	pL4G01	Philco
I3	10	pL4G01	Philco
AR1	27	MEM4000	General Instr.
AR2	27	MEM4000	General Instr.
AR3	27	MEM4000	General Instr.
Q1		2N2222	Texas Instr.
Q2		2N2222	Texas Instr.
Q3		2N2907	Texas Instr.
Q4		2N2222	Texas Instr.
Q5		2N2907	Texas Instr.
CR1		IN916	Texas Instr.
CR2		IN916	Texas Instr.
CR3		IN916	Texas Instr.
CR4		IN916	Texas Instr.
R1		1K ±5% 1/8W	Allen Bradley
R2		5.1K "	"
R3		1K "	"
R4		5.1K "	"
R5		3.3K "	"
R6		24K "	"
R7		6.8K "	"
R8		5.1K "	"
R9		1K "	"

Designation	Location On Schematic Diagram	Part Number			Manufacturer
R10		10K	± 5%	1/8%	Allen Bradley
R11		36K	"		"
R12		20K	"		"
R13		20K	"		"

Appendix F

DIGITAL ADAPTOR FOR TRANSDUCERS

PARTS LIST

TO MANUAL LIMIT ADJUSTMENT BOX

According To Function

Designation	Location on Schematic Diagram	Part Number	Manufacturer
FF1 through 10 (SR10)	1 through 10	MEM1005	General Instr.
FF11	11	MEM1005	General Instr.
A1	12	pL4G01	Philco
OR1	12	pL4G01	Philco
OR2	12	pL4G01	Philco
I	12	pL4G01	Philco
SR40	13, 14	2xMEM3021	General Instr.
Q1		2N2222	Texas Instr.
R1		47K±5% 1/8 W carb.comp.	Allen Bradley
R2		10K±5% 1/8 W carb.comp.	Allen Bradley
R3		1M±5% 1/8 W carb.comp.	Allen Bradley
C1		.1MF±20%35V	Mallory
S1	Lever action switch	6M2412	Mallory
S2	Toggle switch	20994LH	Arrow-Hart
S3	Push-button "tiny"switch	953	Switchcraft
S5	"	"	"
S6 through S15	"	"	"

DIGITAL ADAPTER FOR TRANSDUCERS

PARTS LIST TO MANUAL LIMIT ADJUSTMENT BOX

According to Location on Schematic Diagram

Module Number	Function in Logic Diagram	Part Number	Manufacturer
1	SR10 (FF1)	MEM1005	General Instr.
2	" (FF2)	"	"
3	" (FF3)	"	"
4	" (FF4)	"	"
5	" (FF5)	"	"
6	" (FF6)	"	"
7	" (FF7)	"	"
8	" (FF8)	"	"
9	" (FF9)	"	"
10	" (FF10)	"	"
11	FF11	"	"
12	A1,OR1,OR2,I	pL4G01	Philco
13	SR40	MEM3021	General Instr.
14	SR40	MEM3021	General Instr.

Appendix G

DIGITAL ADAPTOR FOR TRANSDUCERS

PARTS LIST TO CONTROL UNIT

Designation	Part Number	Manufacturer
SC1	pL4C01	Philco
	pL4G02	"
SC2	pL4C01	"
	pL4G02	"
SC3	pL4C01	"
	pL4C01	"
	pL4C01	"
A2	pL4G01	"
A3	"	"
A4	"	"
A5	"	"
A6	"	"
A7	"	"
A8	"	"
A9	"	"
A10	"	"
A11	"	"
A12	"	"
A13	"	"
A14	connection	
A15	pL4G01	"
A16	pL4G01	"
OR1	pL4G01	"

Designation	Part Number	Manufacturer
OR2		
CR_1 through CR_9	IN916	Texas Instr.
Q16	2N2907	Texas Instr.
R16	15K ohm ± 5% 1/8W	Allen Bradley
R17	20K ohm ± 5% 1/8W	Allen Bradley
OR3	pL4601	Philco
OR4	pL4601 (with I)	Philco
F1	MEM1005	General Instr.
F2	MEM1005	General Instr.
F3	MEM1005	General Instr.
SR1	MEM3012SP	General Instr.
AR	MEM4000	General Instr.
I	pL4601 (with OR4)	Philco
Q1	2N2222	Texas Instr.
Q2	2N2907	Texas Instr.
Q3	2N2907	Texas Instr.
Q4	2N2905	Texas Instr.
Q5	2N2907	Texas Instr.
Q6 through Q15	2N2907	Texas Instr.
R1	47K ± 5% 1/8W carbon comp.	Allen Bradley
R2	10K " "	"
R3	1M " "	"
R4	2K " "	"
R5	330 " "	"
R6 through R15	51K " "	"

Appendix G

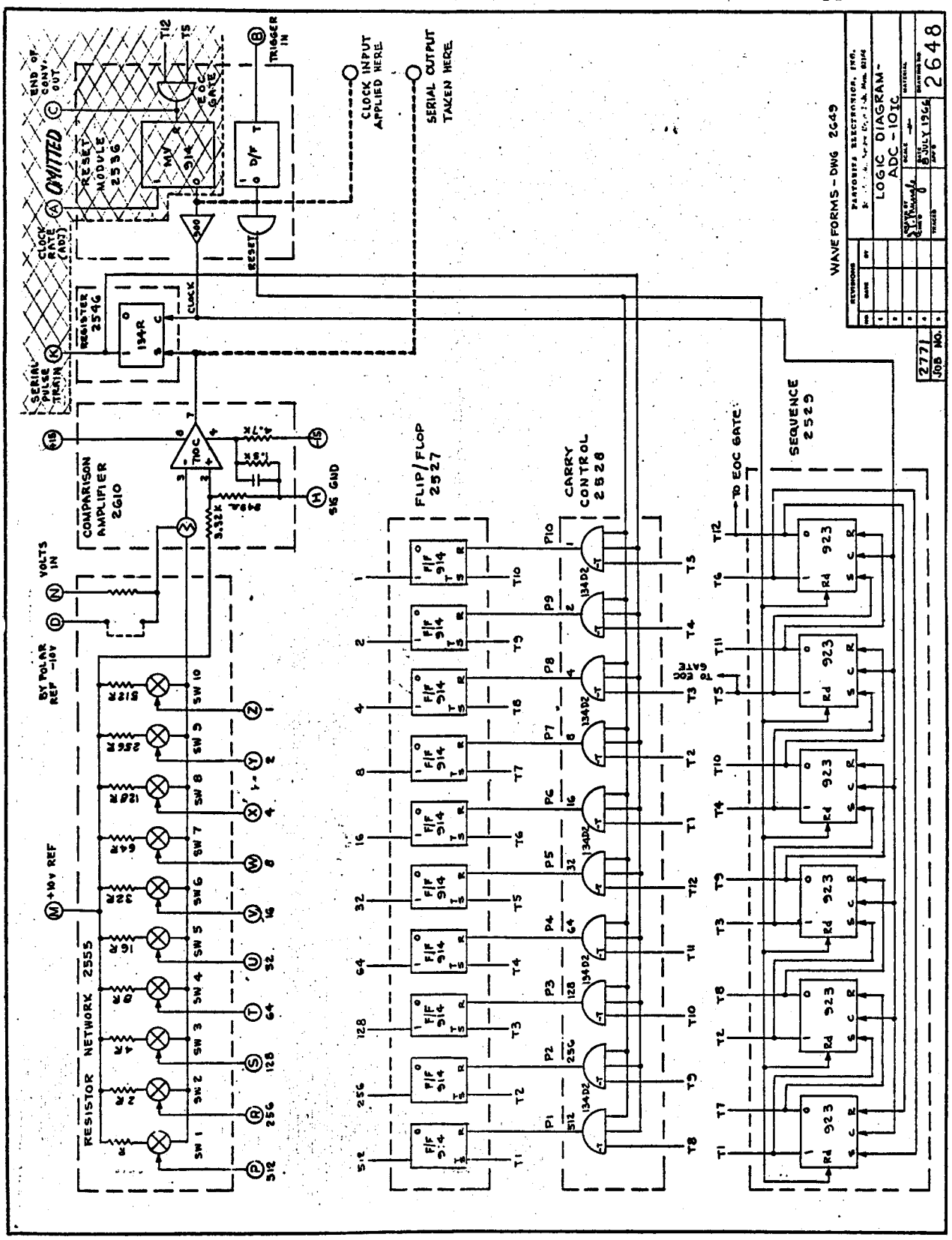
Designation	Part Number	Manufacturer
C1	.68 μF ± 20% 35v	Mallory
P	10 ± 5% 1/4 w carbon potention.	Mallory
B_1 through B_{10}	10V35-45 mA inc. lamp 60D7414 (10ES)	Sylvania
S1	push-button"tiny switch" 953	Switchcraft
S2through S7	toggle switch 20994-Cs	Arrow Hart
S8	rotary switch 1211L	Mallory

1.0 SPECIFICATIONS

Input Impedance	2.4K
Input Voltage	0 to -10 volts
Conversion Command Input	+2 volts 0.2 uSec Rise Time
Conversion Gain	1-bit = 10 mv.
Total Conversion Time	10 uSec.
Resolution	10-bits
Output Format	10 Parallel Voltage Levels 1 Serial Output @ 1 mHz Rate.
Output Logic Levels	False or "0" = 0 to +.2 volts True or "1" = 2 volts.
Output Impedance	470 ohms
Output Current	± 2 mas.
Status Output (EOC)	"1" or True Level when conversion is complete.
Power Supply Requirements	± 15 volts at 20 mas. +4.5 volts at 300 mas.
Linearity	.05% or 1/2 bit
Warm up Drift	10 mv.
Variation with Supply Voltage	¼ volt in +15 causes 10 mv.error 1 volt in -15 causes 10 mv.error 1 volt in +4.5 causes 2 mv.error

Output Code

		MSB									LSB
Unipolar	0,000	=0	0	0	0	0	0	0	0	0	0
	-9,990	=1	1	1	1	1	1	1	1	1	1
Bipolar	+5,000	=0	0	0	0	0	0	0	0	0	0
	0,000	=1	0	0	0	0	0	0	0	0	0
	-4.990	=1	1	1	1	1	1	1	1	1	1


OMITTED
END OF CONV. OUT
RESET MODULE 2536
MV 914 EOC GATE
T12
T5
TRIGGER IN
D/F T
CLOCK INPUT APPLIED HERE
SERIAL OUTPUT TAKEN HERE
CLOCK RATE (ADJ.)
500
RESET
CLOCK
REGISTER 2546
194R
SERIAL PULSE TRAIN
COMPARISON AMPLIFIER 2610
THOC
SIG GND
VOLTS IN
BY POLAR REF -10V
+10v REF
RESISTOR NETWORK 2555
SW 10
SW 9
SW 8
SW 7
SW 6
SW 5
SW 4
SW 3
SW 2
SW 1
FLIP/FLOP 2527
F/F 914
CARRY CONTROL 2528
13402
SEQUENCE 2529
TO EOC GATE
R4 923
WAVE FORMS - DWG 2649
LOGIC DIAGRAM - ADC-10Tc
PHOTOBELL ELECTRONICS, INC.
JULY 1964
2771
JOB NO.
2648